

# **ARCHITETTURA DEI SISTEMI ELETTRONICI**

## **LEZIONE N° 11**

- **Reti sequenziali**
- **Bistabile**
- **Flip - Flop S – R**
- **Flip - Flop S – R Cloccato**
- **D Latch**
- **Temporizzazioni**
- **Durata minima dell'impulso**

**A.S.E.**

**11.1**

## **Richiami**

- **Reti combinatorie**
  - **Porte elementari**
  - **Porte NAND e NOR**
- **Reti sequenziali**
  - **Concetto di cicli**
- **Sintesi delle reti combinatorie**
- **Alee**

**A.S.E.**

**11.2**

## Definizioni

- **Reti COMBINATORIE**
  - In qualunque istante le uscite sono funzione del valore che gli ingressi hanno in quell'istante
  - Il comportamento (uscite in funzione degli ingressi) è descritto da una tabella
- **Reti SEQUENZIALI**
  - In un determinato istante le uscite sono funzione del valore che gli ingressi hanno in quell'istante e i valori che hanno assunto precedentemente
  - La descrizione è più complessa
  - Stati Interni
  - Reti dotate di *MEMORIA*

A.S.E.

11.3

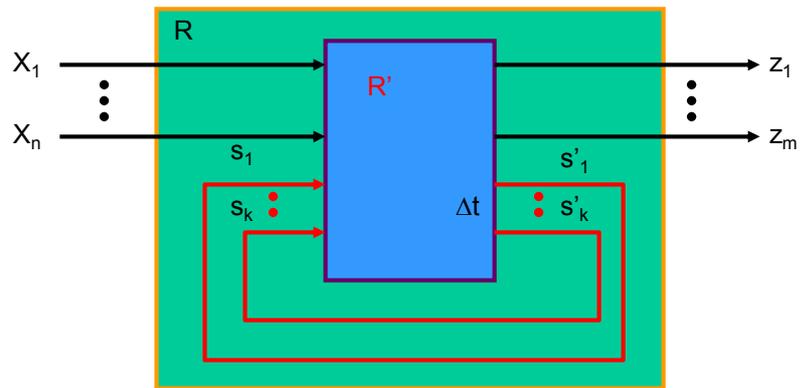
## Memoria delle reti sequenziali

- **Osservazione**
  - In ogni istante la rete deve “ricordarsi” il valore che alcune variabili logiche avevano precedentemente
  - la memorizzazione viene fatta da “opportuni” collegamenti interni alla rete
    - Cicli
    - Anelli di reazione
    - Anelli
- **Attenzione !!**
  - l'assenza di cicli comporta => rete combinatoria
  - la presenza di cicli non garantisce =>reti sequenziali
  - (reazione positiva)

A.S.E.

11.4

## Modello di rete sequenziale

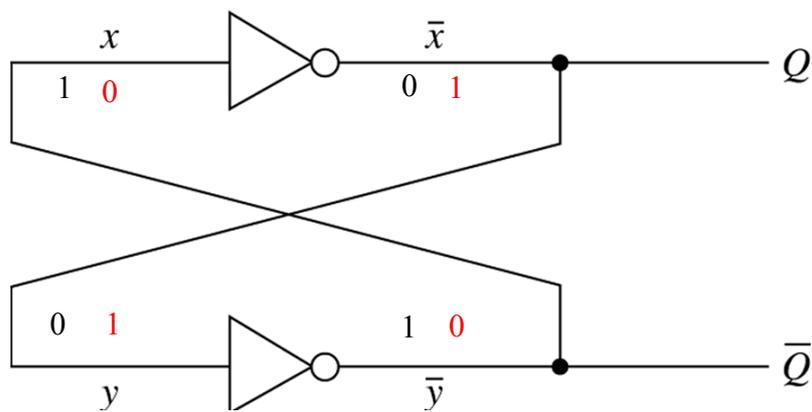


La rete  $R'$  è priva di anelli, ovvero è una rete combinatoria

A.S.E.

11.5

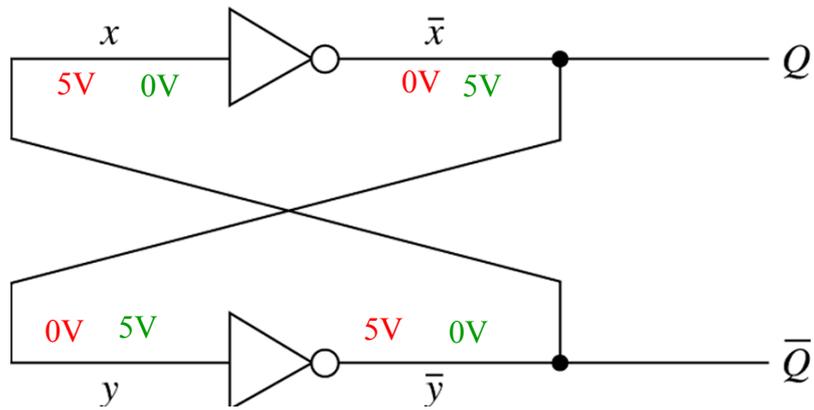
## Elemento di memoria



A.S.E.

11.6

## Bistabile livelli elettrici

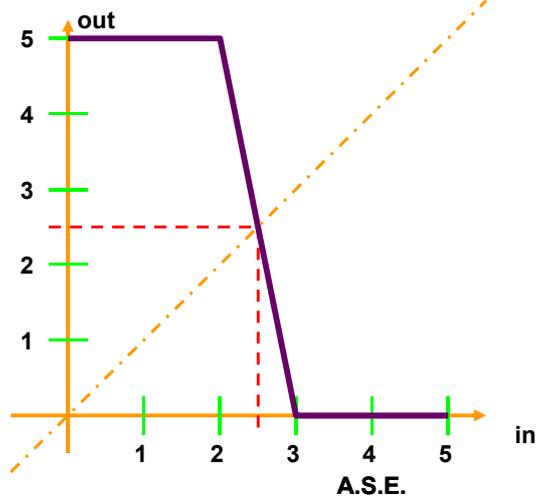


A.S.E.

11.7

## Caratteristica dell'inverter (NOT)

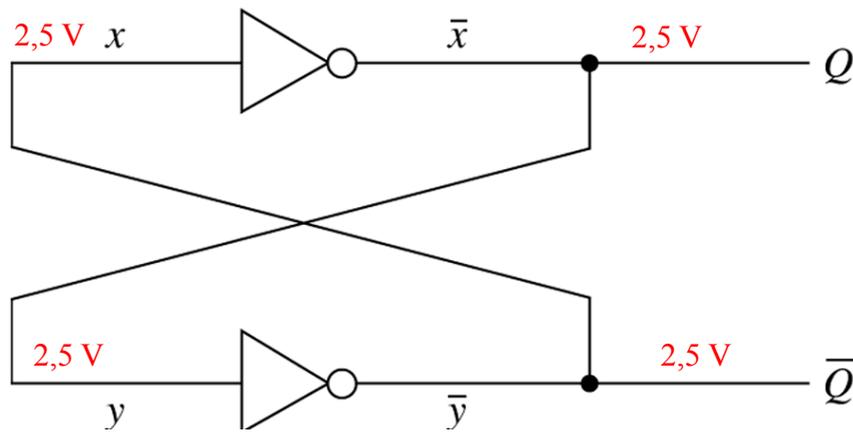
- Caratteristica di trasferimento



A.S.E.

11.8

## Metastabilità



A.S.E.

11.9

## Osservazioni 1

- Il Bistabile non ha ingressi
- Il valore delle uscite viene determinato all'accensione
- Rimane stabile fin quando alimentato
- FLIP – FLOP => bistabile con ingressi
- **Setting** o **Presetting** => Uscita a "1"
- **Resetteing** o **Clearing** => Uscita a "0"

A.S.E.

11.10

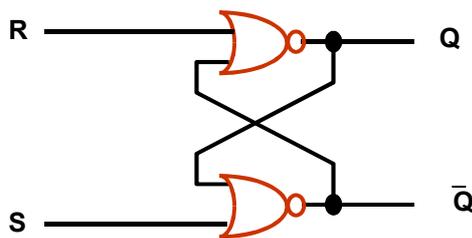
## Osservazioni 2

- Gli ingressi di un FLIP – FLOP sono di 2 tipi
  - **Asincroni** o ingressi diretti
    - Il F-F cambia stato immediatamente
  - **Sincroni**
    - Il F-F risponde di tali ingressi quando sono attivi altri segnali di controllo chiamati **CLOCK** o **ENABLE** (abilitatore)
- Flip – Flop **LATCH** => classe di F-F tali che
  - L'uscita risponde immediatamente ad una variazione degli'ingressi

A.S.E.

11.11

## Flip – Flop SR



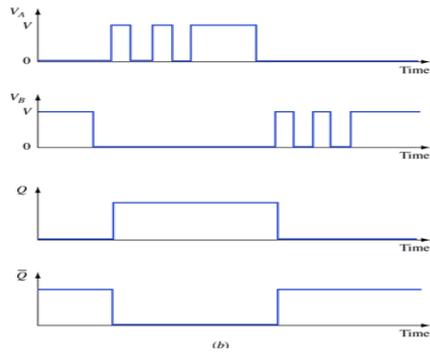
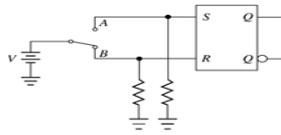
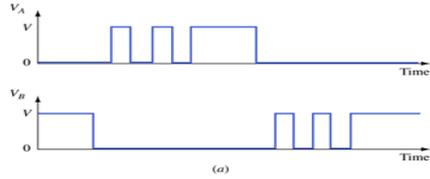
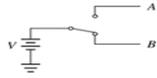
S	R	Q <sup>+</sup>	Q̄ <sup>+</sup>
0	0	Q	Q̄
0	1	0	1
1	0	1	0
1	1	-	-

S = R = 1 => condizione proibita

A.S.E.

14.12

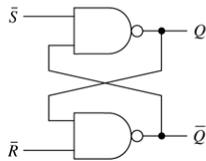
## Esempio = Antirimbalzi



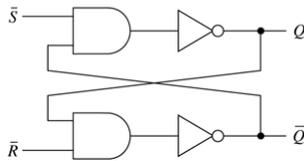
A.S.E.

11.13

## Flip - Flop $\bar{S} \bar{R}$



(a)



(b)

Inputs		Outputs	
$\bar{S}$	$\bar{R}$	$Q^+$	$\bar{Q}^+$
0	0	1*	1*
0	1	1	0
1	0	0	1
1	1	$Q$	$\bar{Q}$

\*Unpredictable behavior will result if inputs return to 1 simultaneously

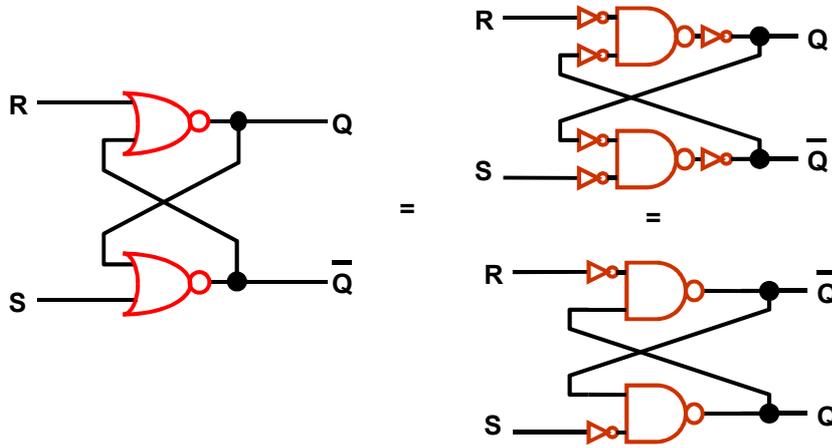


(c)

A.S.E.

11.14

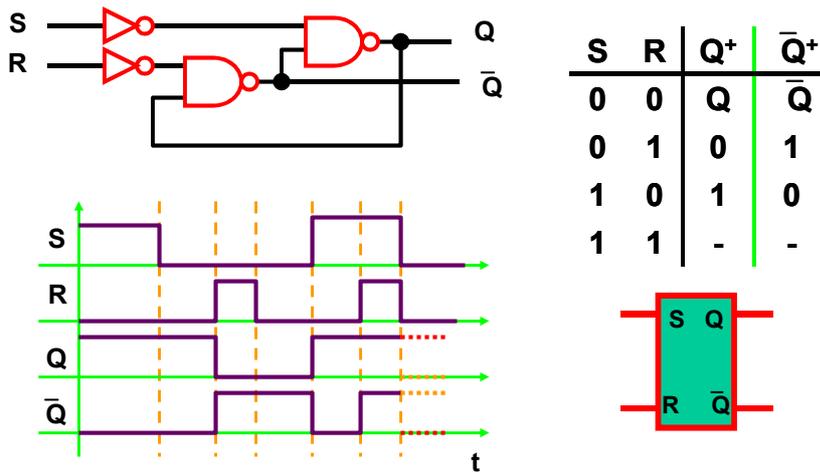
## Flip – Flop SR ( Teorema di De Morgan)



A.S.E.

14.15

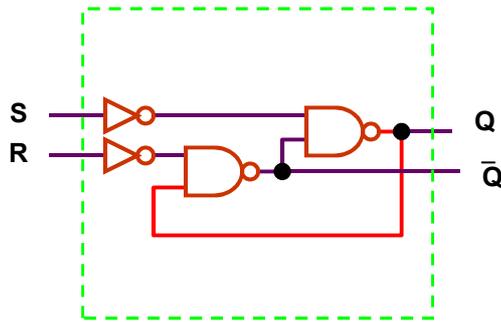
## Flip – Flop S-R alternativo



A.S.E.

11.16

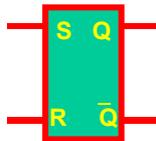
## Schema circuitale



A.S.E.

11.17

## Simbolo



A.S.E.

11.18

## Tabella delle funzioni (delle transizioni)

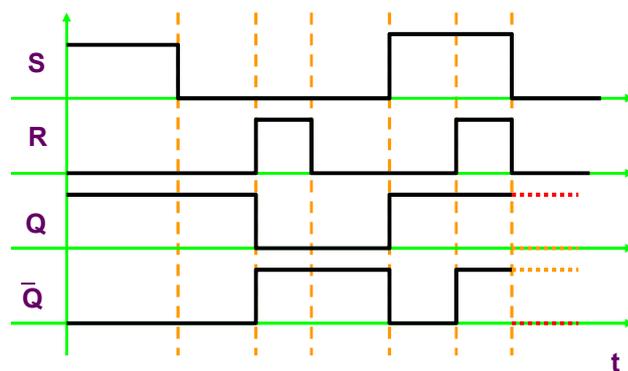
S	R	Q <sup>+</sup>	$\bar{Q}$ <sup>+</sup>
0	0	Q	$\bar{Q}$
0	1	0	1
1	0	1	0
1	1	-	-

Stato successivo    (Stato futuro)  
Stato Presente

A.S.E.

11.19

## Forme d'onda

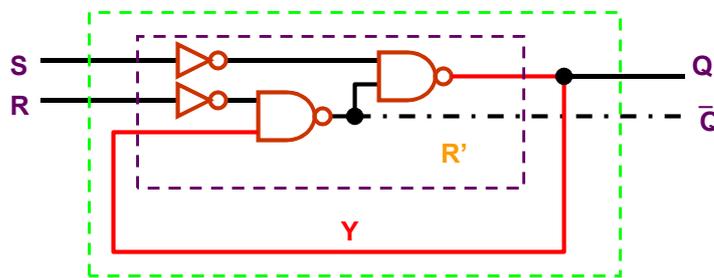


A.S.E.

11.20

## Variabili di stato

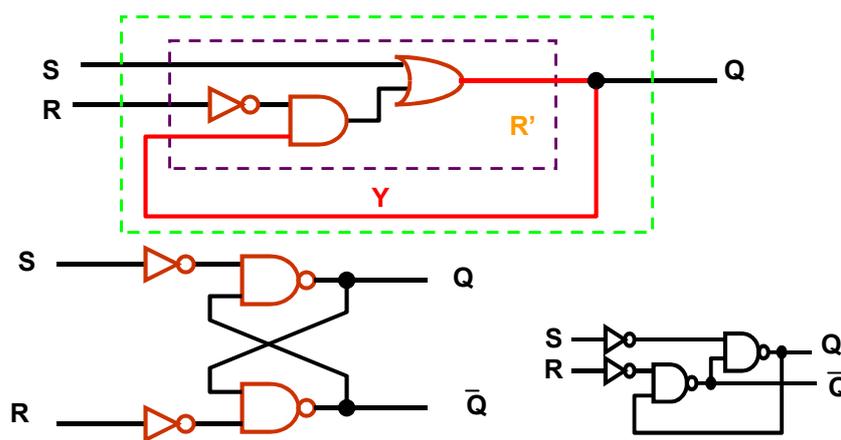
- La capacità di “memorizzazione è legata agli anelli di richiusura interni
  - Variabili di stato
  - Tante quante sono le richiuse “k”
  - Stati interni  $2^k$



A.S.E.

11.21

## Altre rappresentazioni del F- F [S-R]



A.S.E.

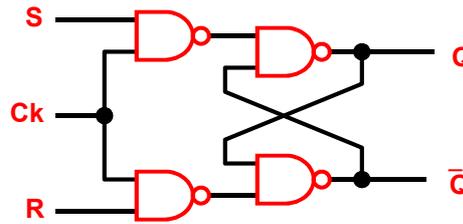
11.22

## Flip – Flop S – R con abilitazione

• Tabella delle funzioni

Schema

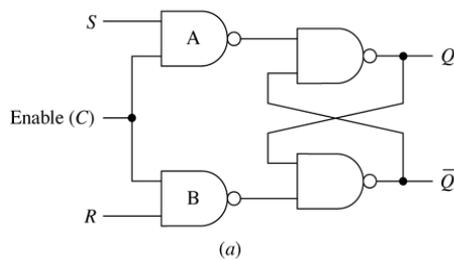
Ck	S	R	Q <sup>+</sup>	$\bar{Q}^+$
0	x	x	Q	$\bar{Q}$
1	0	0	Q	$\bar{Q}$
1	0	1	0	1
1	1	0	1	0
1	1	1	-	-



A.S.E.

11.23

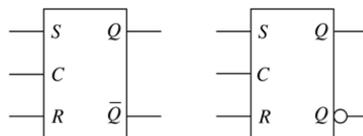
## Flip – Flop SR “cloccato” 2



Inputs			Outputs	
S	R	C	Q <sup>+</sup>	$\bar{Q}^+$
0	0	1	Q	$\bar{Q}$
0	1	1	0	1
1	0	1	1	0
1	1	1	1*	1*
X	X	0	Q	$\bar{Q}$

\*Unpredictable behavior will result if S and R return to 0 simultaneously or C returns to 0 while S and R are 1

(b)

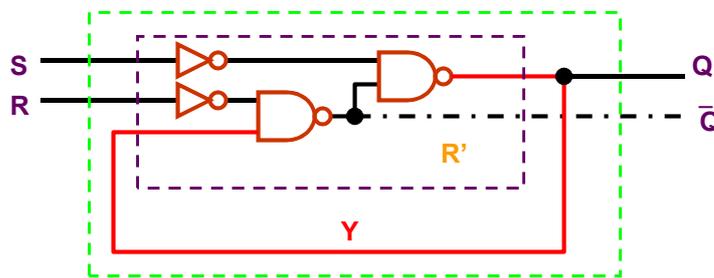


A.S.E.

11.24

## Variabili di stato

- La capacità di “memorizzazione è legata agli anelli di richiusura interni
  - Variabili di stato
  - Tante quante sono le richiuse “k”
  - Stati interni  $2^k$



A.S.E.

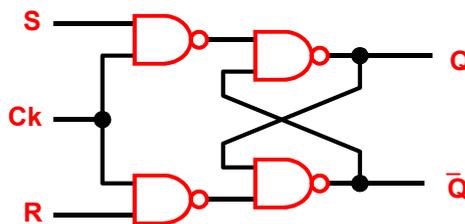
11.25

## Flip – Flop S – R con abilitazione

- Tabella delle funzioni

Schema

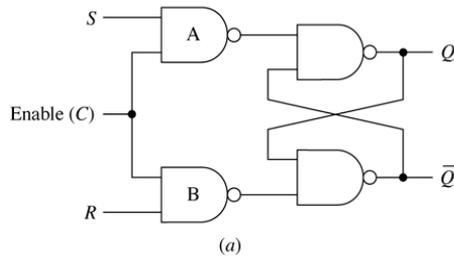
Ck	S	R	Q <sup>+</sup>	Q̄ <sup>+</sup>
0	x	x	Q	Q̄
1	0	0	Q	Q̄
1	0	1	0	1
1	1	0	1	0
1	1	1	-	-



A.S.E.

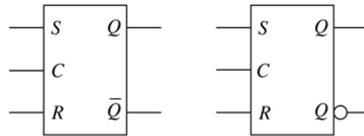
11.26

## Flip – Flop SR “cloccato” 2



Inputs			Outputs	
S	R	C	$Q^+$	$\bar{Q}^+$
0	0	1	$Q$	$\bar{Q}$
0	1	1	0	1
1	0	1	1	0
1	1	1	1*	1*
X	X	0	$Q$	$\bar{Q}$

\*Unpredictable behavior will result if S and R return to 0 simultaneously or C returns to 0 while S and R are 1



A.S.E.

11.27

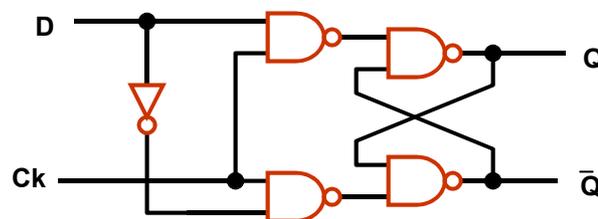
## Flip – Flop **D LATCH**

- Per  $Ck = 1$ 
  - L'uscita Q segue l'ingresso D
- Per  $Ck = 0$ 
  - L'uscita conserva lo stato precedente

• Tabella delle funzioni

Ck	D	$Q^+$
0	x	Q
1	0	0
1	1	1

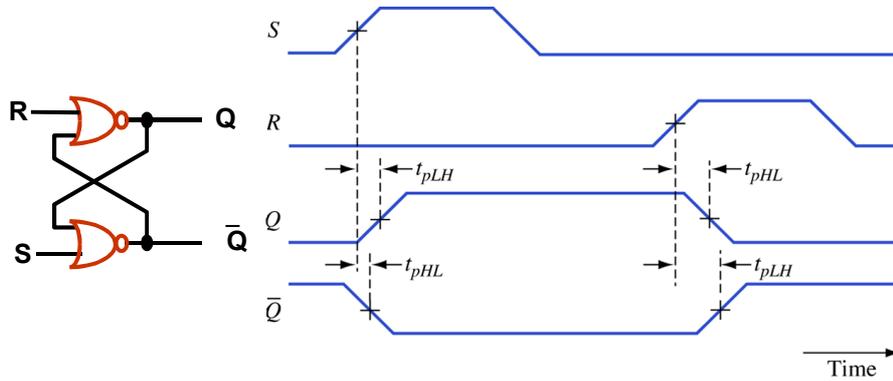
Schema



A.S.E.

11.28

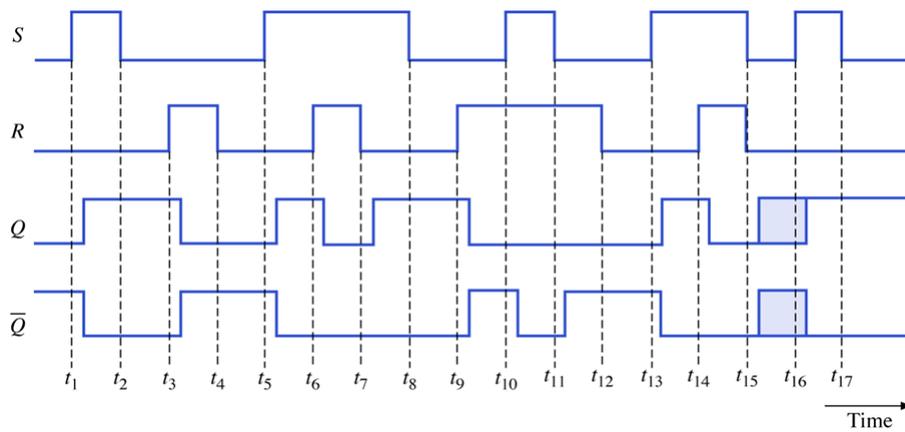
## Tempi di propagazione



A.S.E.

11.29

## Temporizzazione schematica

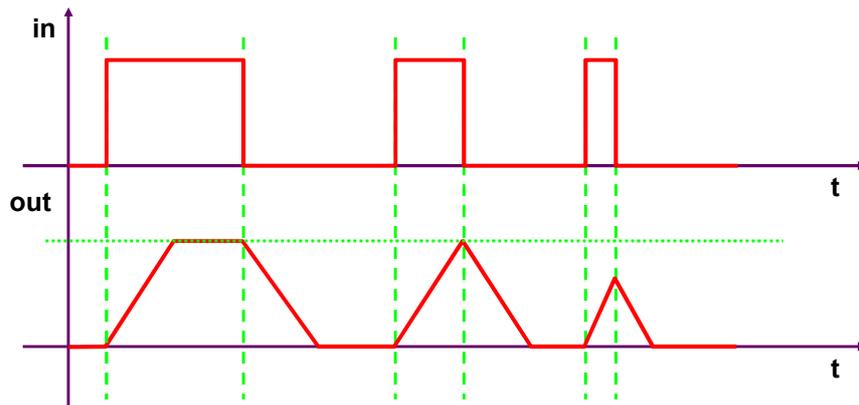


A.S.E.

11.30

## Durata minima dell'impulso 1

- Forme d'onda di una rete combinatoria

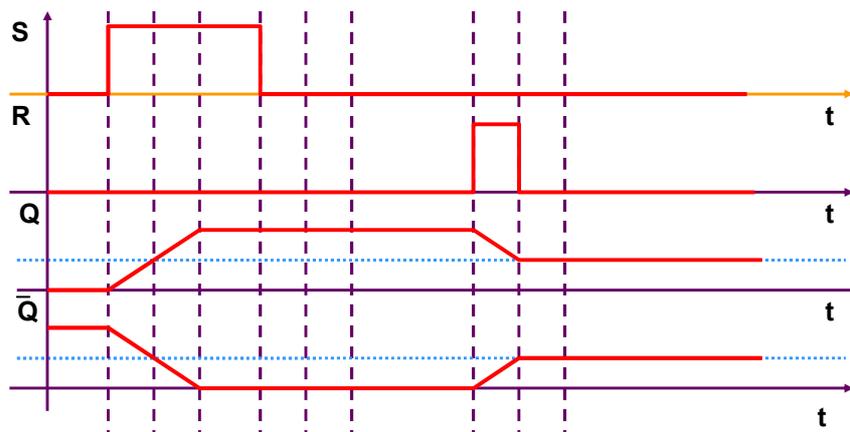


A.S.E.

11.31

## Durata minima dell'impulso 2

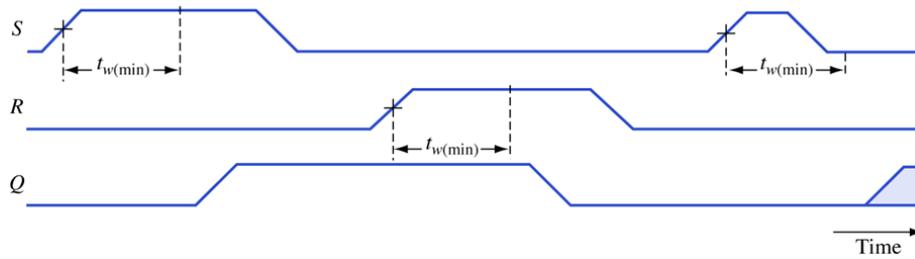
- Forme d'onda di un Flip – Flop SR



A.S.E.

11.32

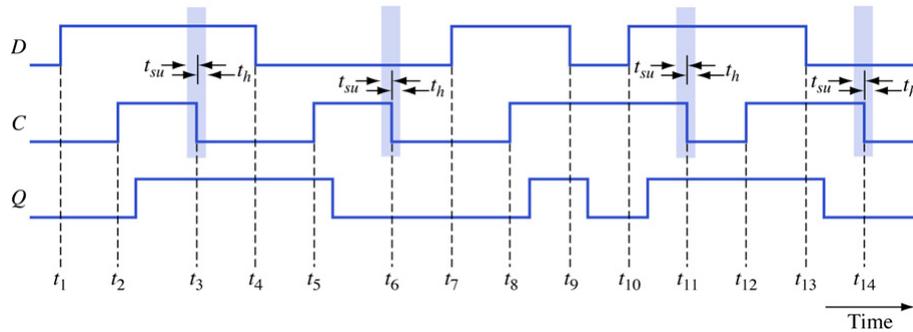
### Durata minima dell'impulso 3



A.S.E.

11.33

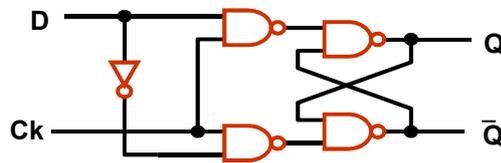
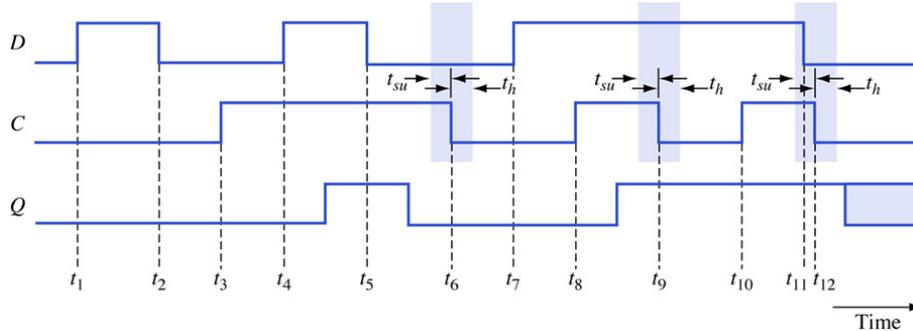
### Tempi di Setup e Hold 1



A.S.E.

11.34

## Tempi di Setup e Hold 2

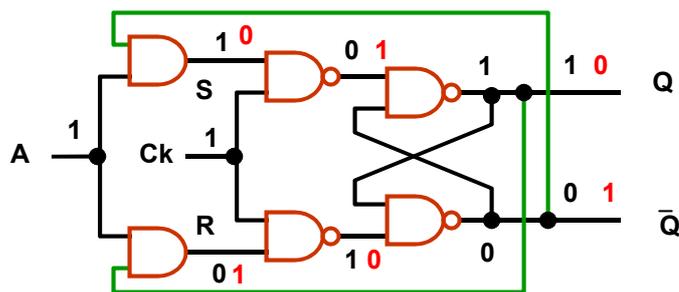


A.S.E.

11.35

## Problema dell'instabilità

- Presenza di anelli multipli

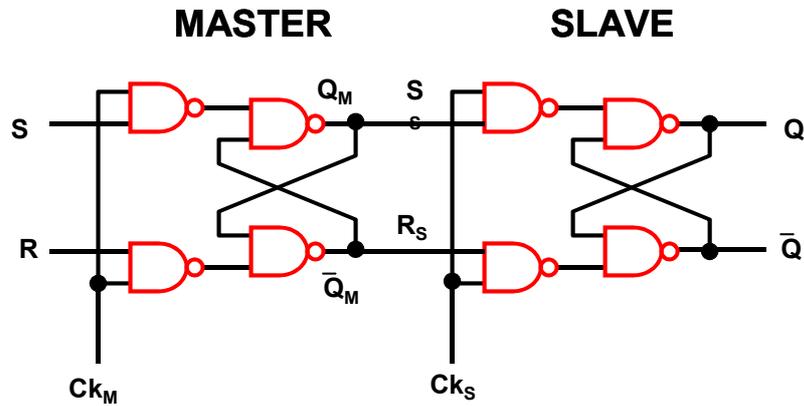


- A causa dei ritardi sulle porte le uscite oscillano

A.S.E.

11.36

## Architettura MASTER - SLAVE

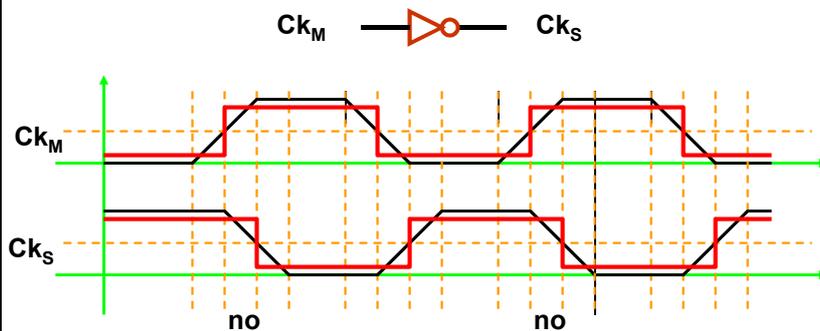


A.S.E.

11.37

## Clock non sovrapposto

- Il clock master e il clock slave non devono mai essere attivi (alti, = 1) contemporaneamente
- Non possono essere ottenuti con un inverter

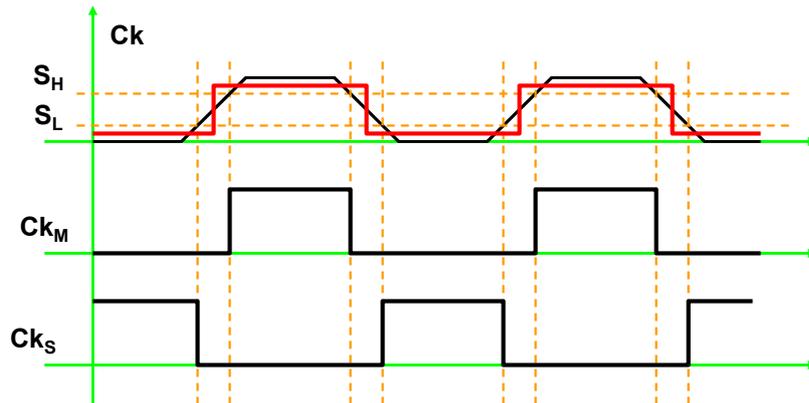


A.S.E.

11.38

## Clock a due fasi non sovrapposte

- Tecnica di generazione a soglia

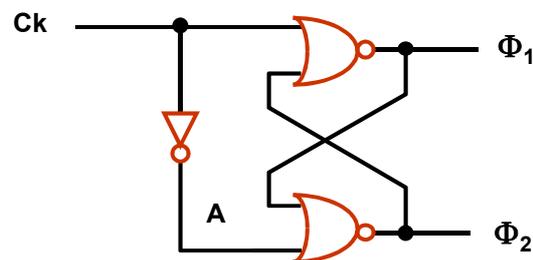


A.S.E.

11.39

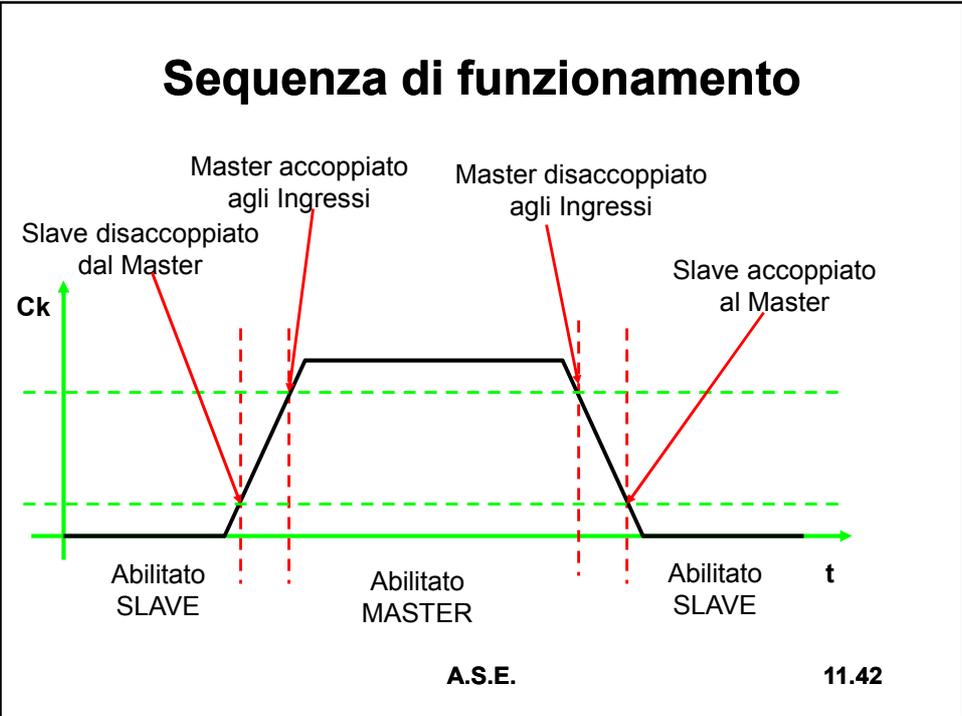
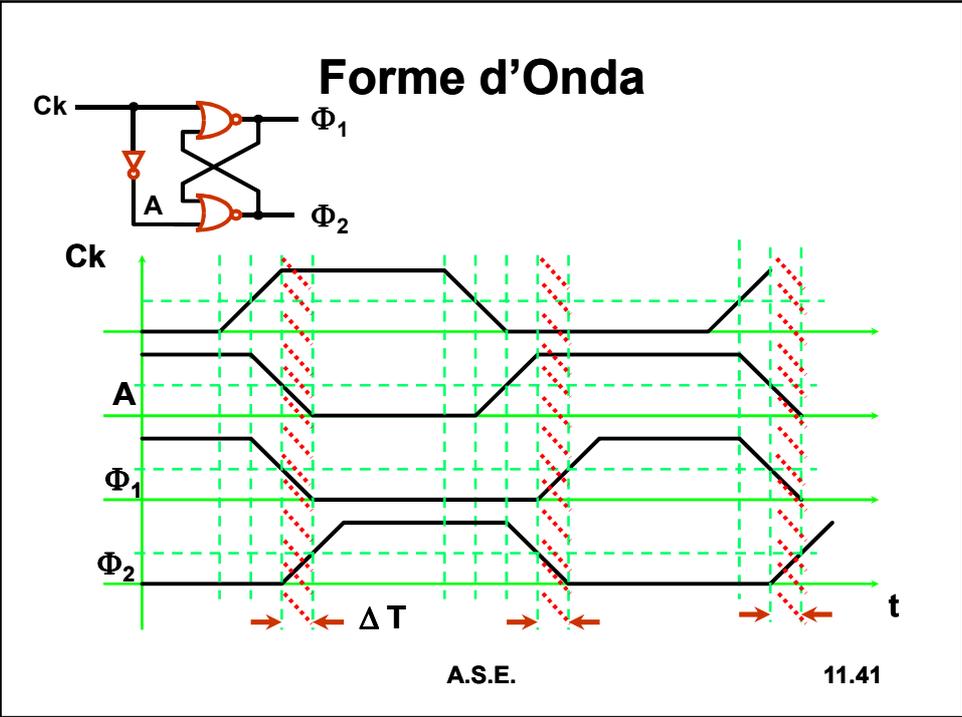
## Generatore di clock a due fasi

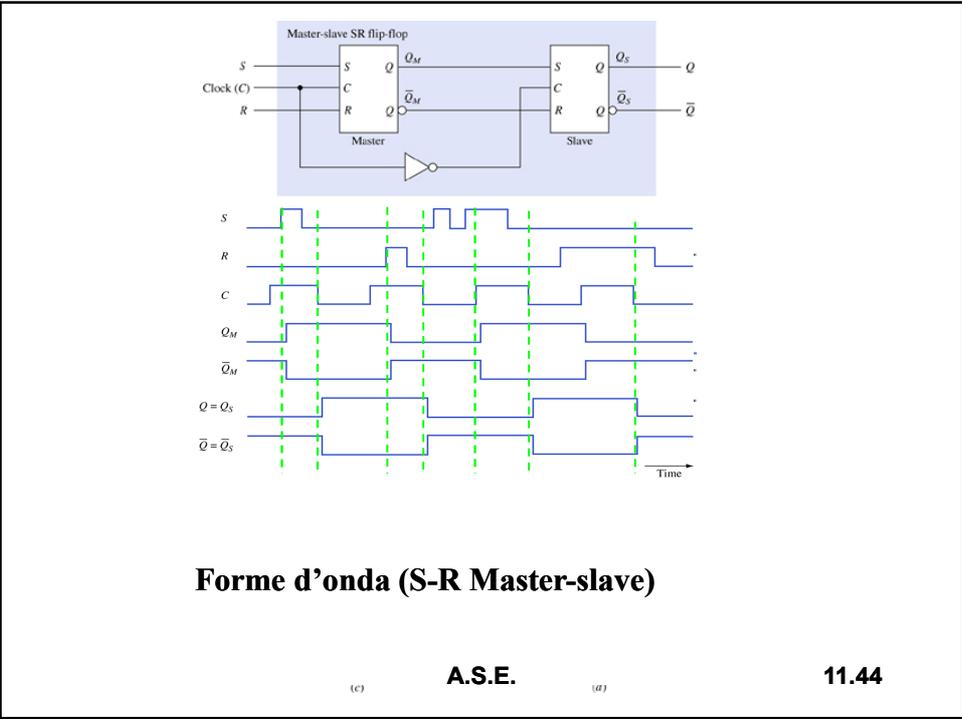
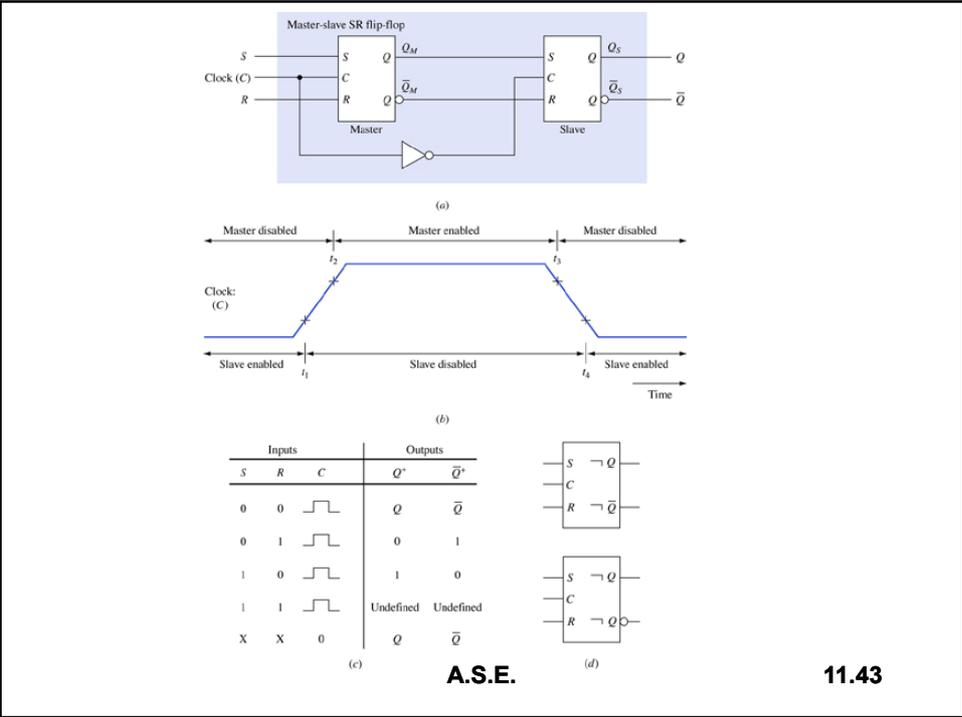
- Un altro modo di generare il Clock a due fasi non sovrapposte



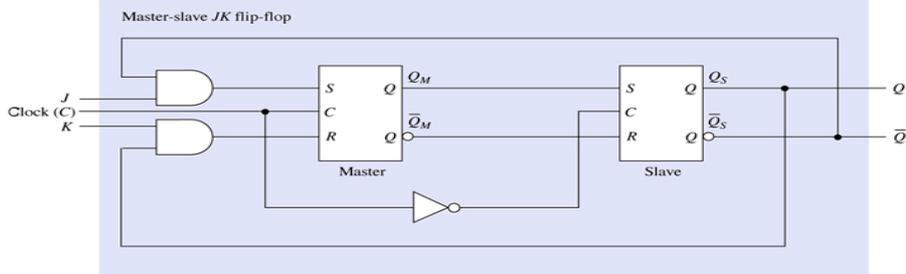
A.S.E.

11.40





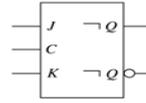
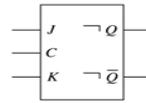
## Flip-flop J – K master-slave



(a)

Inputs			Outputs	
J	K	C	Q <sup>+</sup>	Q <sup>+</sup> -
0	0		Q	Q-bar
0	1		0	1
1	0		1	0
1	1		Q-bar	Q
X	X	0	Q	Q-bar

(b)

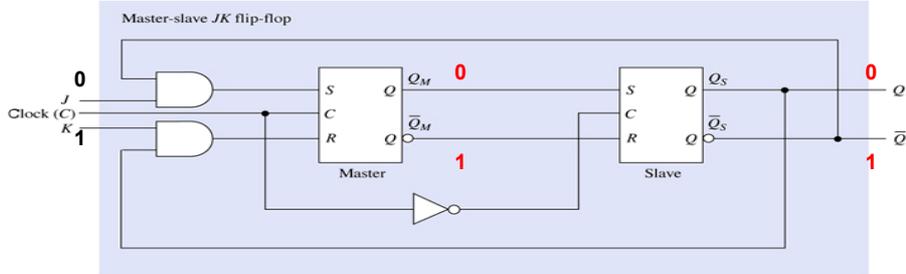


(c)

A.S.E.

11.45

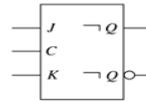
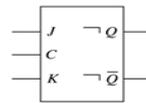
## Flip-flop J – K master-slave



(a)

Inputs			Outputs	
J	K	C	Q <sup>+</sup>	Q <sup>+</sup> -
0	0		Q	Q-bar
0	1		0	1
1	0		1	0
1	1		Q-bar	Q
X	X	0	Q	Q-bar

(b)

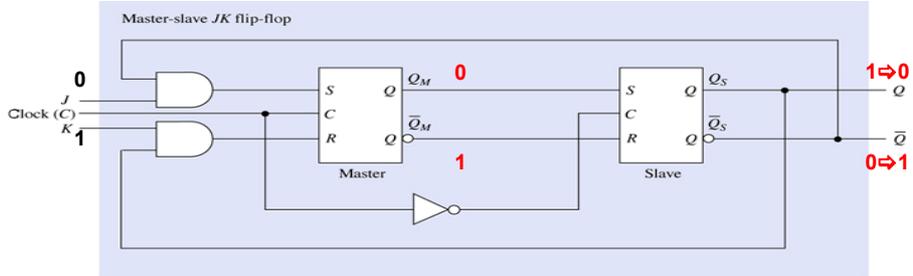


(c)

A.S.E.

11.46

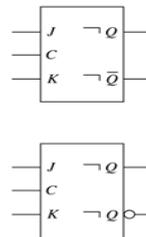
## Flip-flop J – K master-slave



(a)

Inputs			Outputs	
J	K	C	Q <sup>+</sup>	Q <sup>+</sup>
0	0		Q	Q-bar
0	1		0	1
1	0		1	0
1	1		Q-bar	Q
X	X	0	Q	Q-bar

(b)

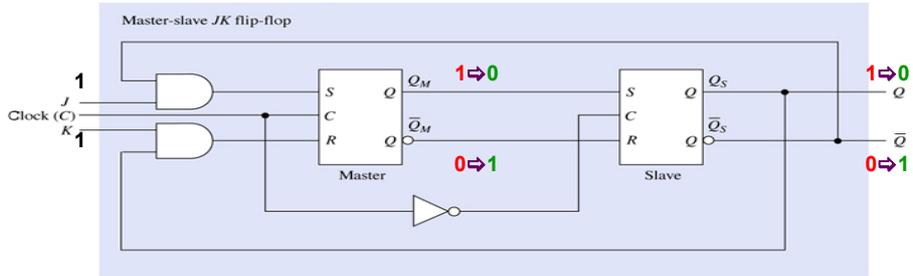


(c)

A.S.E.

11.47

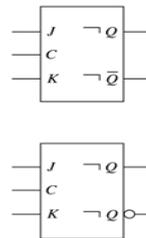
## Flip-flop J – K master-slave



(a)

Inputs			Outputs	
J	K	C	Q <sup>+</sup>	Q <sup>+</sup>
0	0		Q	Q-bar
0	1		0	1
1	0		1	0
1	1		Q-bar	Q
X	X	0	Q	Q-bar

(b)

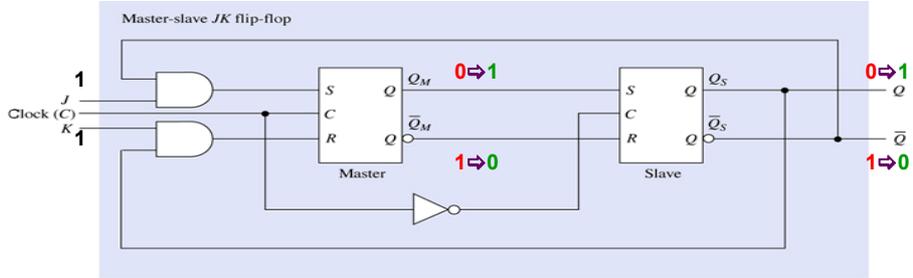


(c)

A.S.E.

11.48

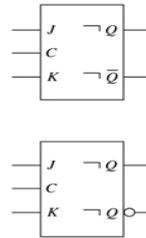
## Flip-flop J – K master-slave



(a)

Inputs			Outputs	
J	K	C	Q <sup>+</sup>	Q <sup>+</sup>
0	0	↑	Q	Q̄
0	1	↑	0	1
1	0	↑	1	0
1	1	↑	Q̄	Q
X	X	0	Q	Q̄

(b)

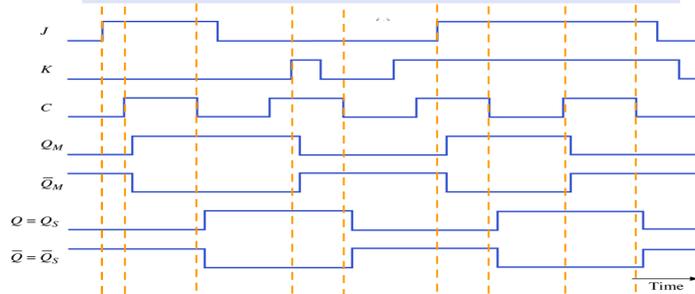
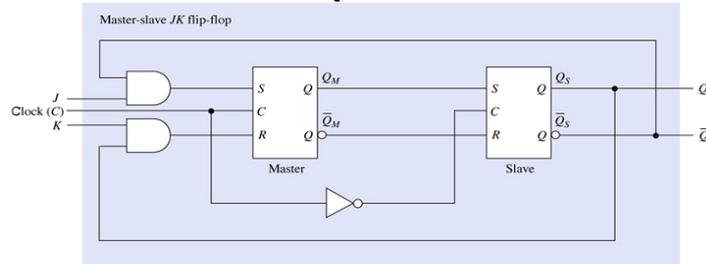


(c)

A.S.E.

11.49

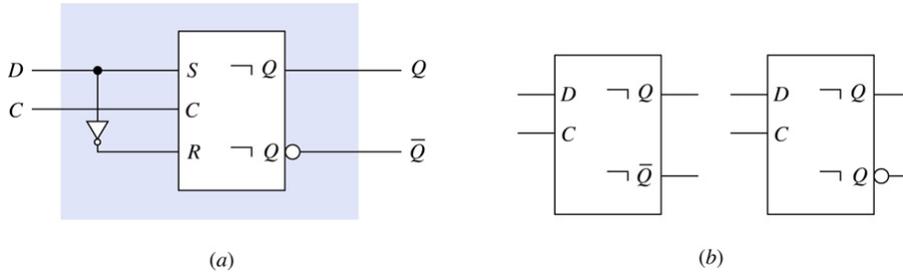
## Forme d'onda (J-K master-slave)



A.S.E.

11.50

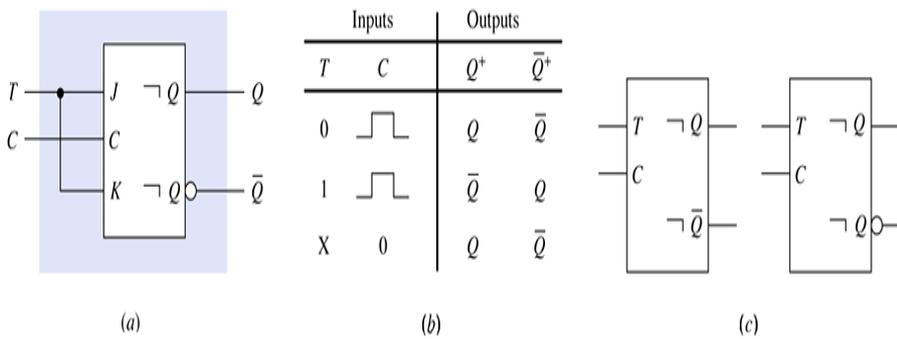
## D Master - Slave



A.S.E.

11.51

## T Master - Slave



A.S.E.

11.52

## **Conclusioni**

- **Reti sequenziali**
- **Bistabile**
- **Flip - Flop S – R**
- **Flip - Flop S – R Cloccato**
- **D Latch**
- **Temporizzazioni**
- **Durata minima dell'impulso**

**A.S.E.**

**11.53**