

# **ARCHITETTURA DEI SISTEMI ELETTRONICI**

## **LEZIONE N° 12**

- **Tempi di Setup e Hold**
- **Architettura MASTER – SLAVE**
- **Clock a 2 fasi**
- **Flip-flop J – K master-slave**
- **Flip-flop D Master - Slave**
- **Flip-flop T Master – Slave**
- **Flip-flop D Edge triggered**
- **Tempi di rispetto**
- **Soluzioni alternative**

**A.S.E.**

**12.1**

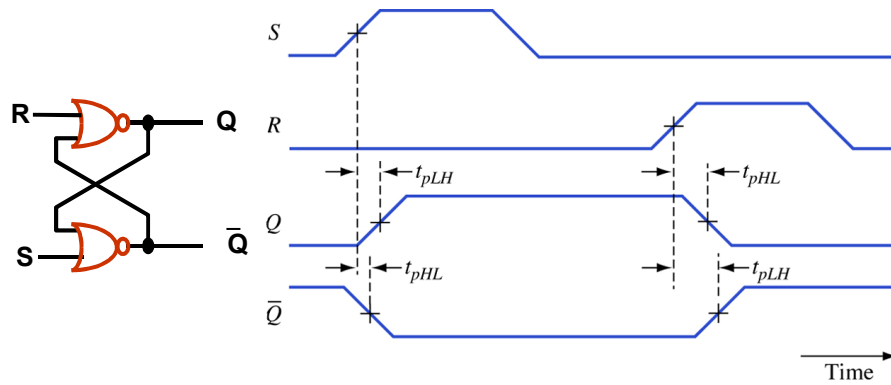
## **Richiami**

- **Reti sequenziali**
- **Bistabile**
- **Flip - Flop S – R, Flip - Flop S – R Cloccato**
- **D Latch**
- **Temporizzazioni**

**A.S.E.**

**12.2**

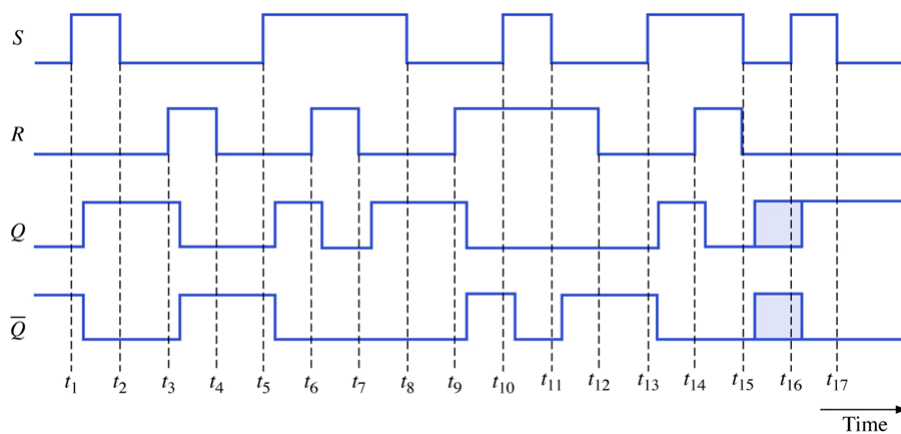
## Tempi di propagazione



A.S.E.

12.3

## Temporizzazione schematica

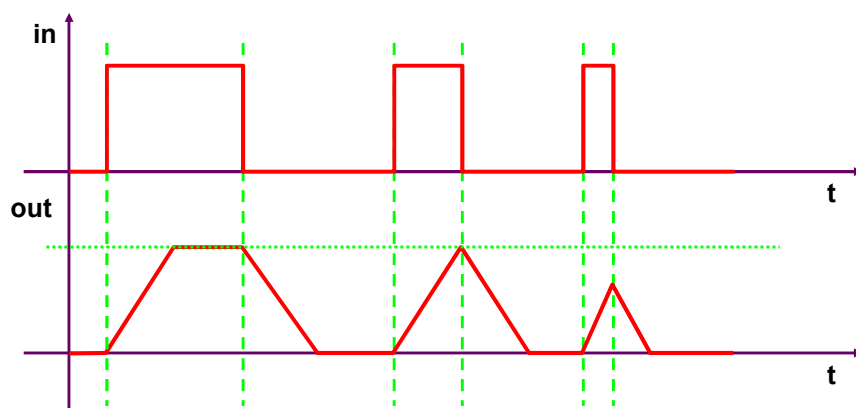


A.S.E.

12.4

## Durata minima dell'impulso 1

- Forme d'onda di una rete combinatoria

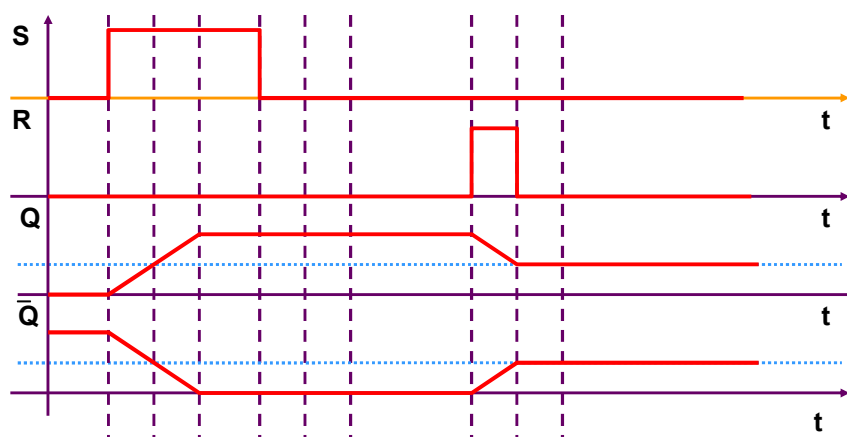


A.S.E.

12.5

## Durata minima dell'impulso 2

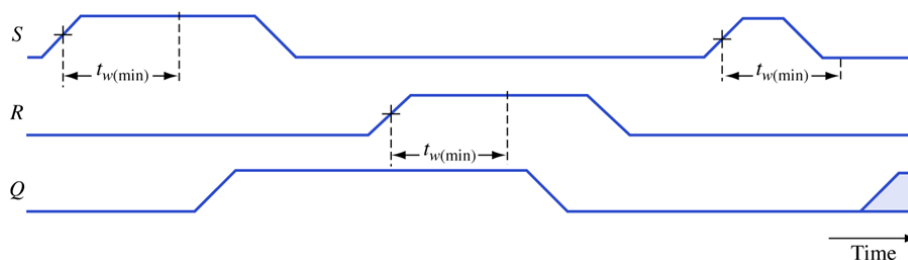
- Forme d'onda di un Flip – Flop SR



A.S.E.

12.6

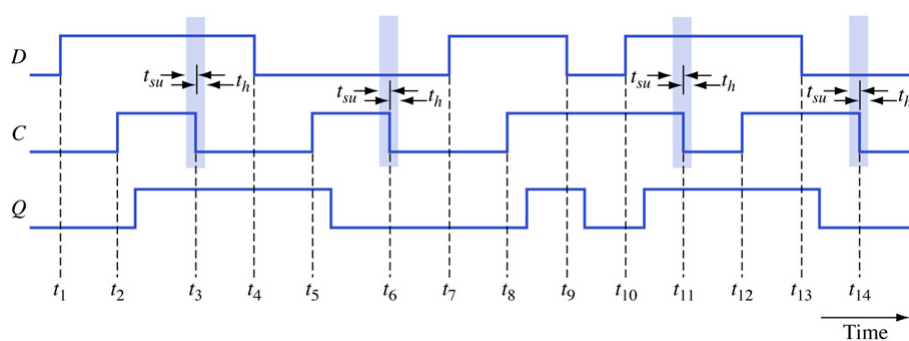
## Durata minima dell'impulso 3



A.S.E.

12.7

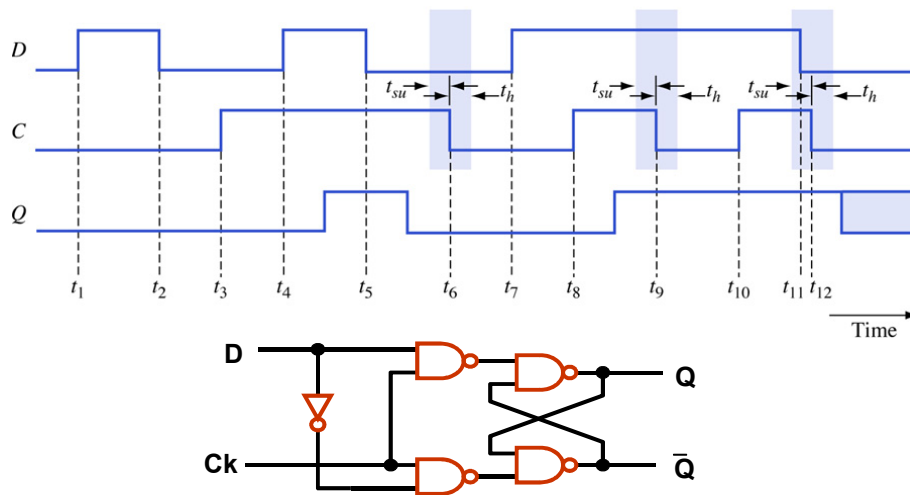
## Tempi di Setup e Hold 1



A.S.E.

12.8

## Tempi di Setup e Hold 2

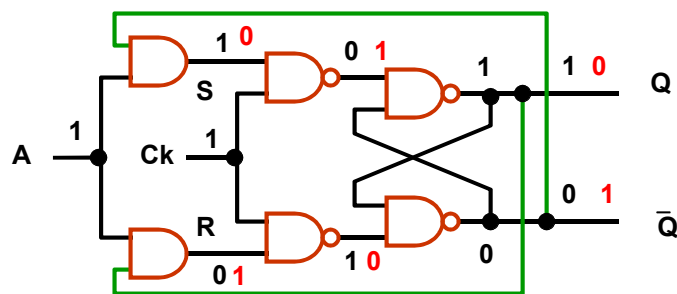


A.S.E.

12.9

## Problema dell'instabilità

- Presenza di anelli multipli

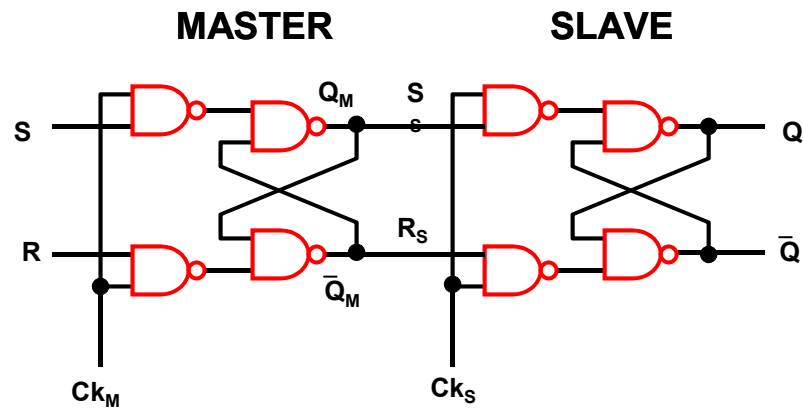


- A causa dei ritardi sulle porte le uscite oscillano

A.S.E.

12.10

## Architettura MASTER - SLAVE

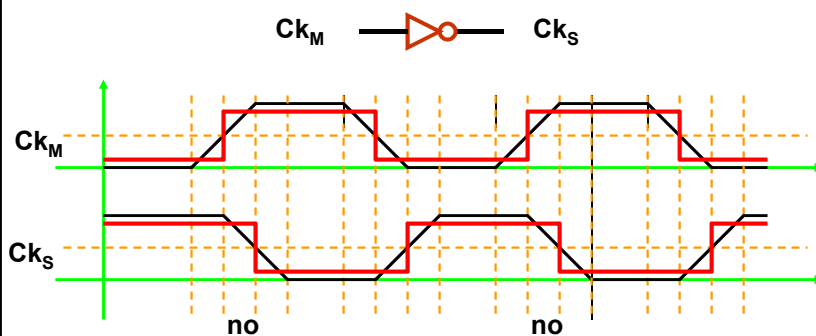


A.S.E.

12.11

## Clock non sovrapposto

- Il clock master e il clock slave non devono mai essere attivi (alti, = 1) contemporaneamente
- Non possono essere ottenuti con un inverter

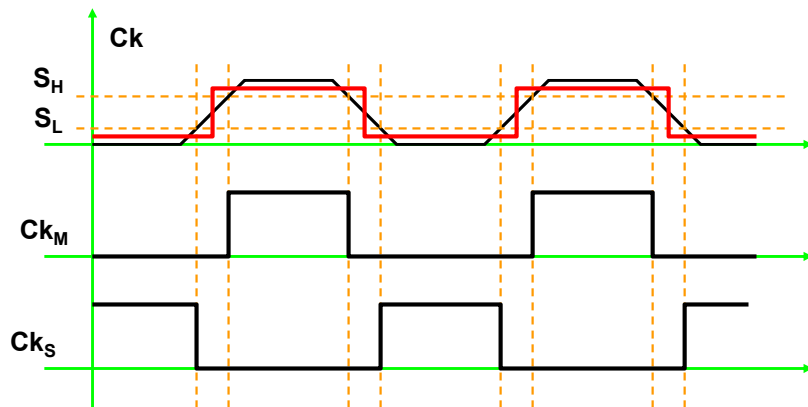


A.S.E.

12.12

## Clock a due fasi non sovrapposte

- Tecnica di generazione a soglia

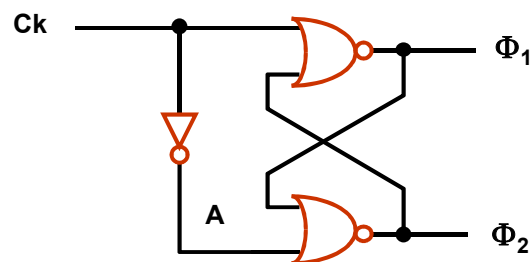


A.S.E.

12.13

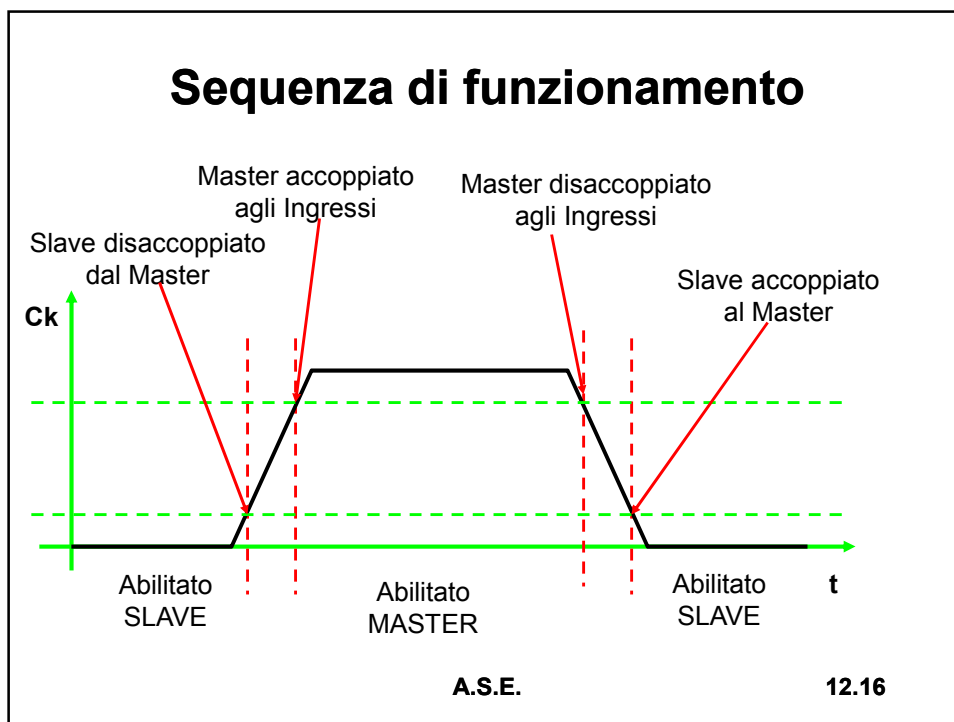
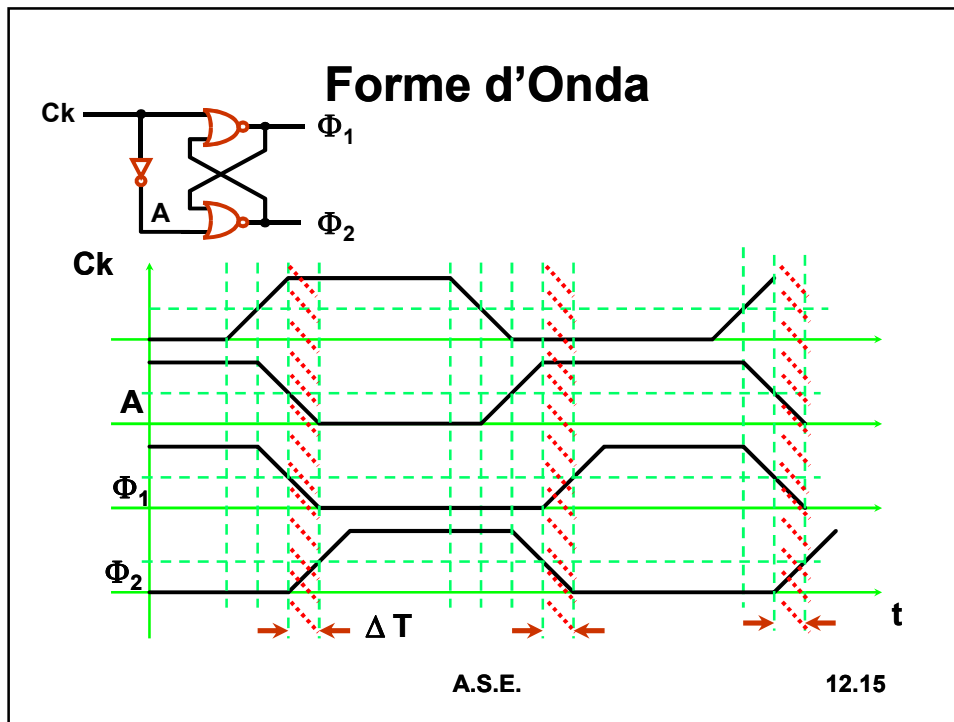
## Generatore di clock a due fasi

- Un altro modo di generare il Clock a due fasi non sovrapposte

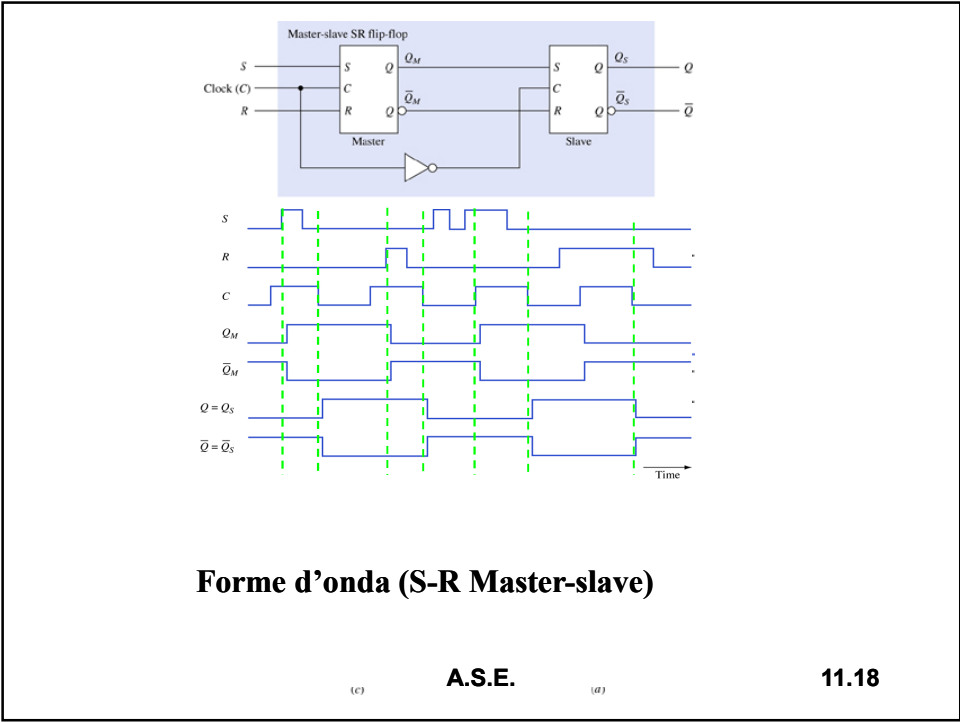
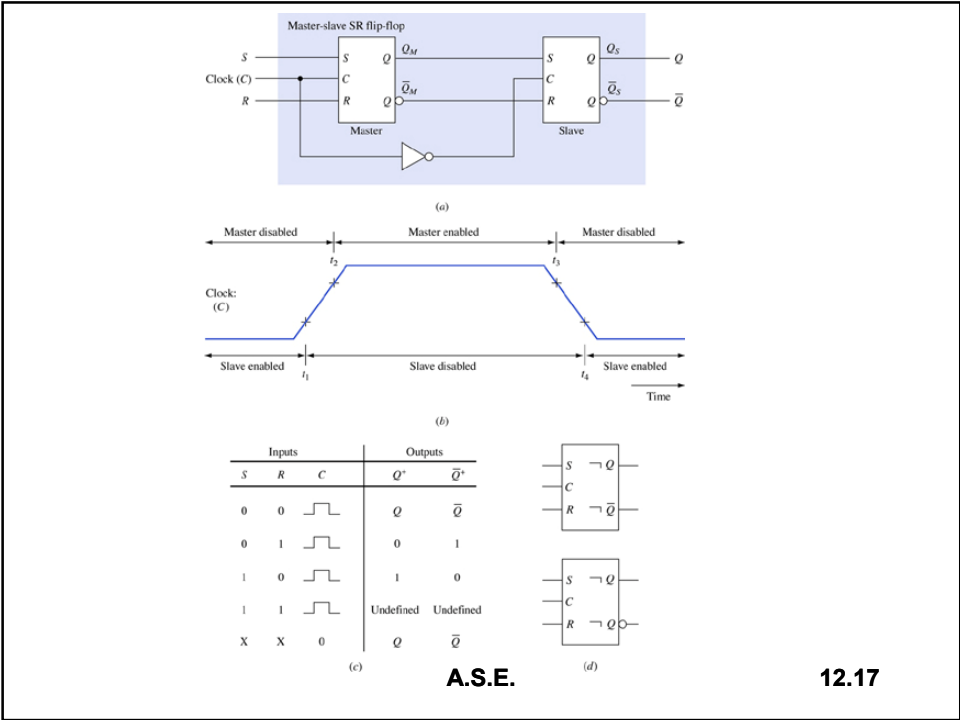


A.S.E.

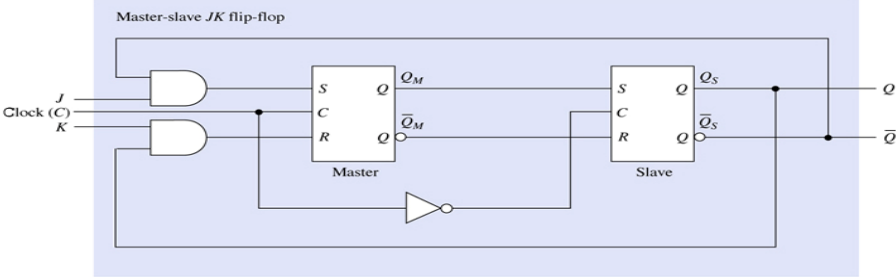
12.14







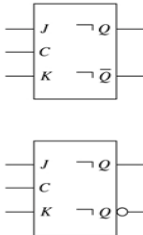
# Flip-flop J – K master-slave



(a)

Inputs			Outputs	
J	K	C	$Q^+$	$\bar{Q}^+$
0	0		Q	$\bar{Q}$
0	1		0	1
1	0		1	0
1	1		$\bar{Q}$	Q
x	x	0	Q	$\bar{Q}$

(b)

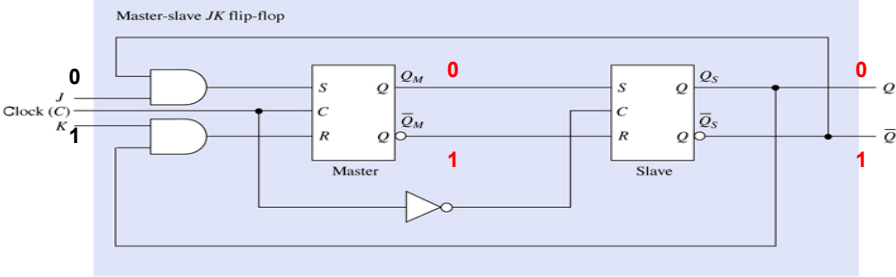


(c)

A.S.E.

11.19

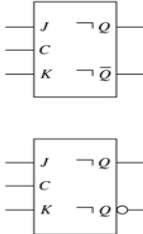
# Flip-flop J – K master-slave



(a)

Inputs			Outputs	
J	K	C	$Q^+$	$\bar{Q}^+$
0	0		Q	$\bar{Q}$
0	1		0	1
1	0		1	0
1	1		$\bar{Q}$	Q
x	x	0	Q	$\bar{Q}$

(b)

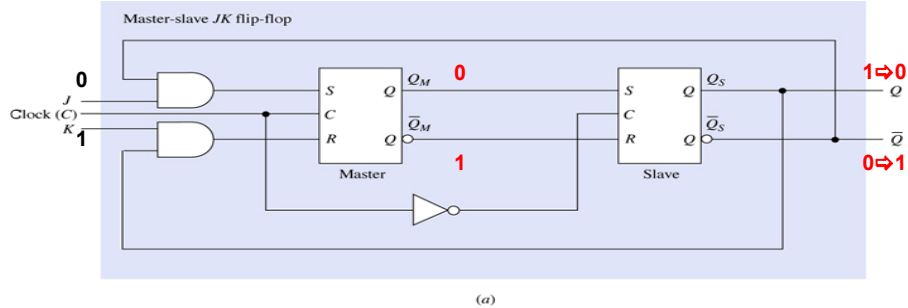


(c)

A.S.E.

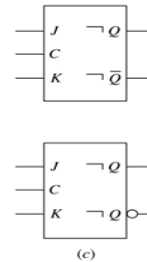
11.20

## Flip-flop J – K master-slave



Inputs			Outputs	
J	K	C	$Q^+$	$\bar{Q}^+$
0	0		Q	$\bar{Q}$
0	1		0	1
1	0		1	0
1	1		$\bar{Q}$	Q
x	x	0	Q	$\bar{Q}$

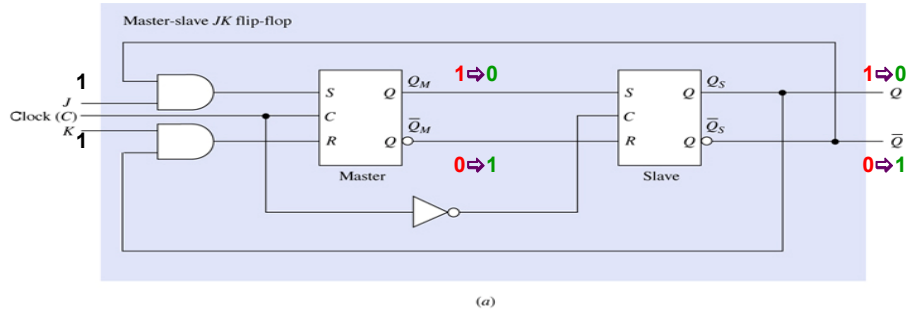
(b)



A.S.E.

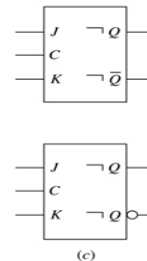
11.21

## Flip-flop J – K master-slave



Inputs			Outputs	
J	K	C	$Q^+$	$\bar{Q}^+$
0	0		Q	$\bar{Q}$
0	1		0	1
1	0		1	0
1	1		$\bar{Q}$	Q
x	x	0	Q	$\bar{Q}$

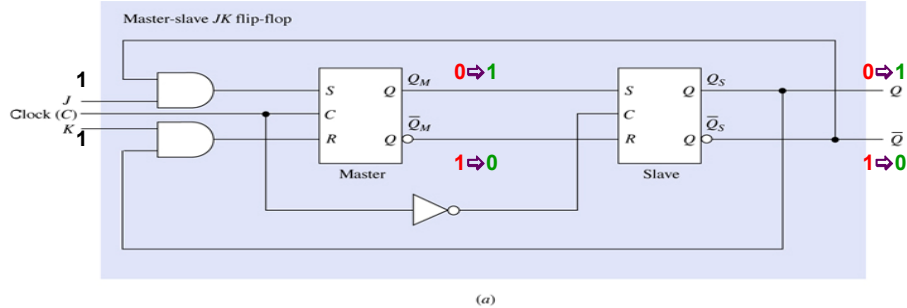
(b)



A.S.E.

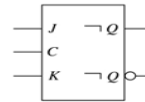
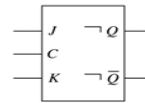
11.22

## Flip-flop J – K master-slave



Inputs			Outputs	
J	K	C	$Q^+$	$\bar{Q}^+$
0	0	0	$Q$	$\bar{Q}$
0	1	0	0	1
1	0	0	1	0
1	1	0	$\bar{Q}$	$Q$
x	x	1	$Q$	$\bar{Q}$

(b)

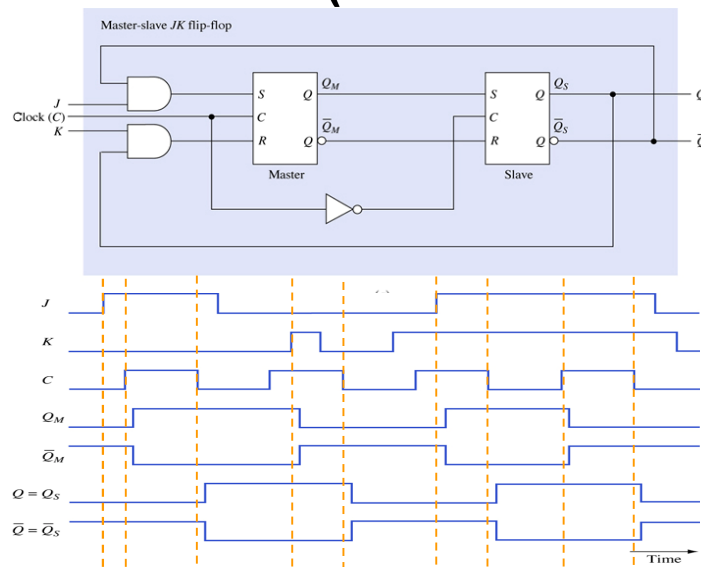


(c)

A.S.E.

11.23

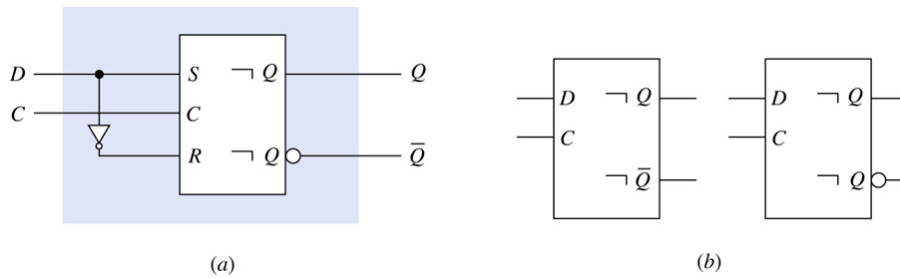
## Forme d'onda (J-K master-slave)



A.S.E.

11.24

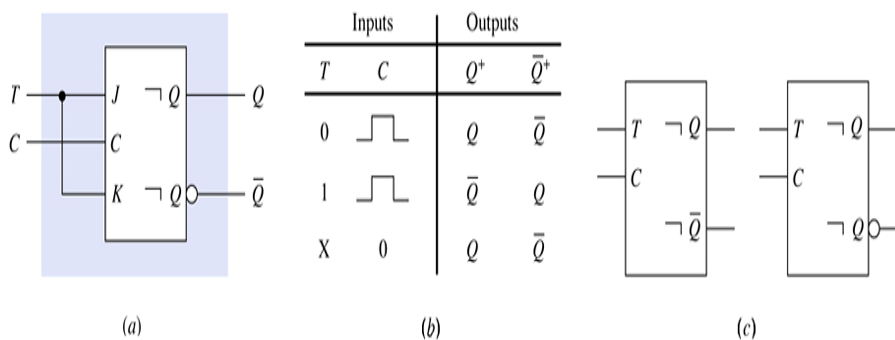
## D Master - Slave



A.S.E.

12.25

## T Master – Slave



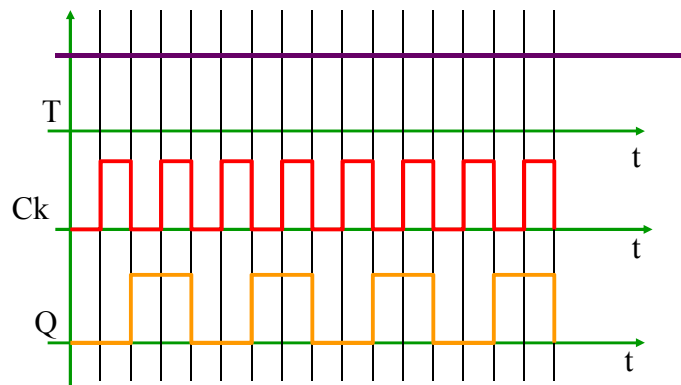
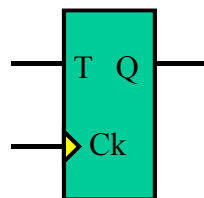
A.S.E.

12.26

## Forme d'onda

•

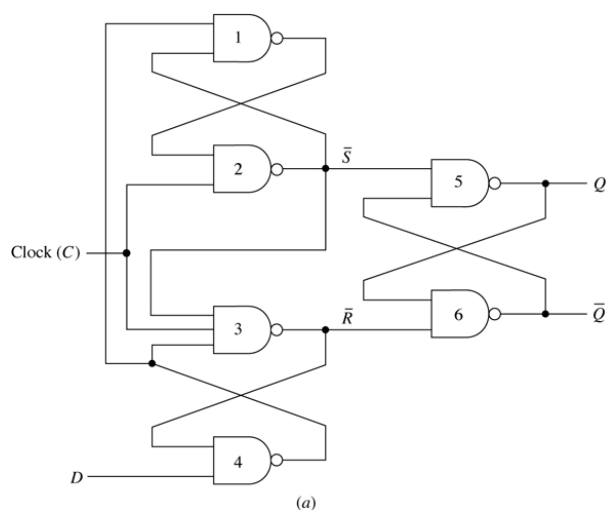
T	Ck	Q <sup>+</sup>
0		Q
1		$\overline{Q}$
X	0	Q



A.S.E.

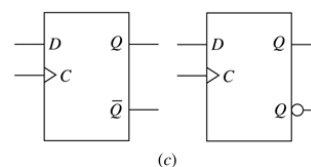
12.27

## Flip-flop D Edge Triggered



Inputs		Outputs	
D	C	Q <sup>+</sup>	$\overline{Q}^+$
0	↑	0	1
1	↑	1	0
X	0	Q	$\overline{Q}$
X	1	Q	$\overline{Q}$

(b)

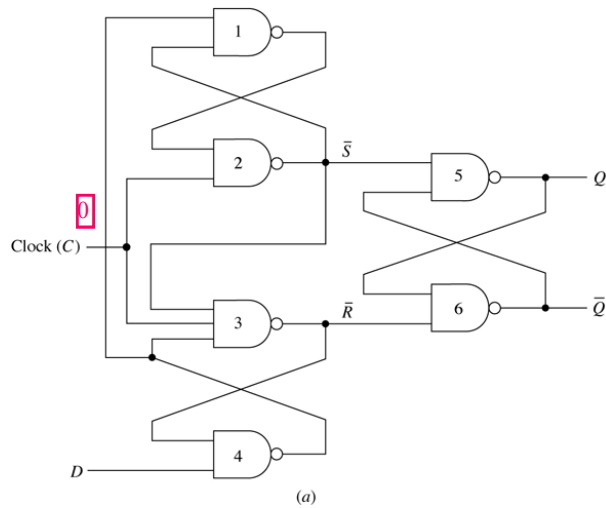


(c)

A.S.E.

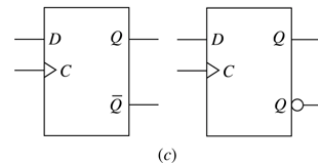
12.28

**(Ck=0)**



Inputs		Outputs	
D	C	$Q^+$	$\bar{Q}^+$
0	↑	0	1
1	↑	1	0
X	0	$Q$	$\bar{Q}$
X	1	$Q$	$\bar{Q}$

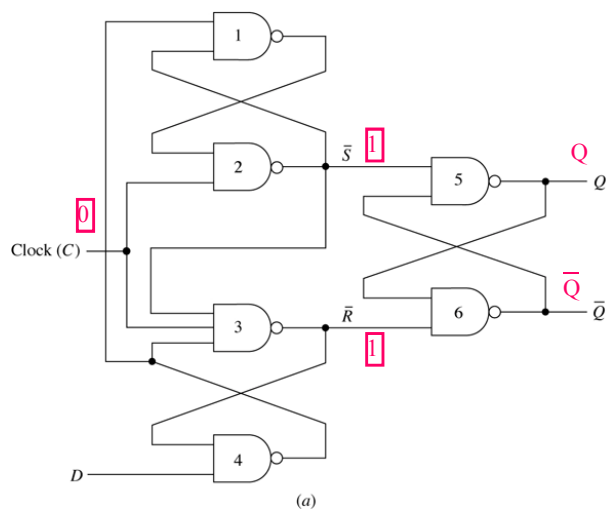
(b)



**A.S.E.**

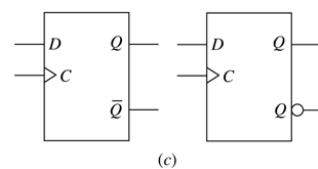
**12.29**

**Ck=0, Q -  $\bar{Q}$**



Inputs		Outputs	
D	C	$Q^+$	$\bar{Q}^+$
0	↑	0	1
1	↑	1	0
X	0	$Q$	$\bar{Q}$
X	1	$Q$	$\bar{Q}$

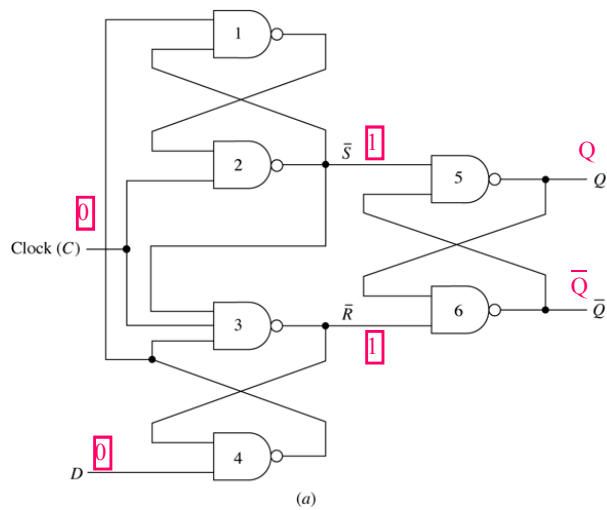
(b)



**A.S.E.**

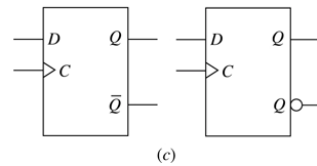
**12.30**

## Ck=0 , D=0 (1)



Inputs		Outputs	
D	C	$Q^+$	$\bar{Q}^+$
0	↑	0	1
1	↑	1	0
X	0	$Q$	$\bar{Q}$
X	1	$Q$	$\bar{Q}$

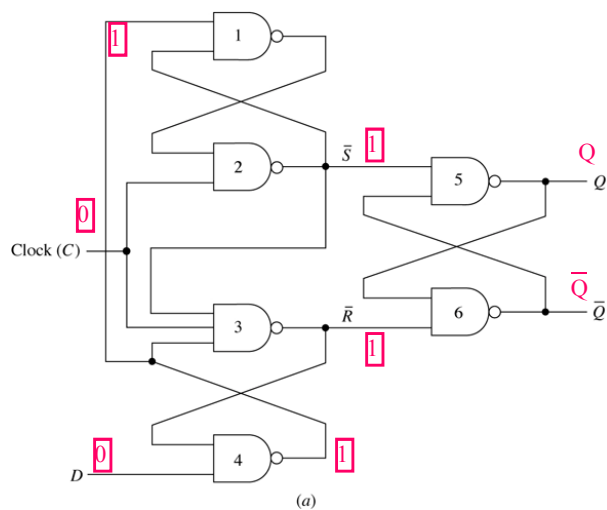
(b)



A.S.E.

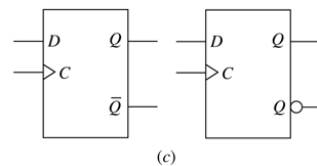
12.31

## Ck=0 , D=0 (2)



Inputs		Outputs	
D	C	$Q^+$	$\bar{Q}^+$
0	↑	0	1
1	↑	1	0
X	0	$Q$	$\bar{Q}$
X	1	$Q$	$\bar{Q}$

(b)

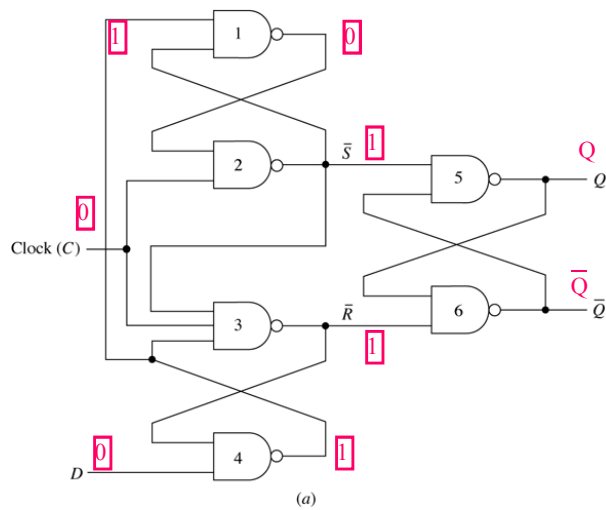


A.S.E.

12.32

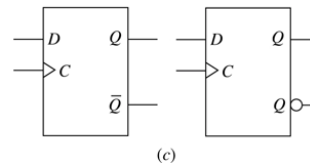


## Ck=0 , D=0 (Fine)



Inputs		Outputs	
D	C	$Q^+$	$\bar{Q}^+$
0	↑	0	1
1	↑	1	0
X	0	$Q$	$\bar{Q}$
X	1	$Q$	$\bar{Q}$

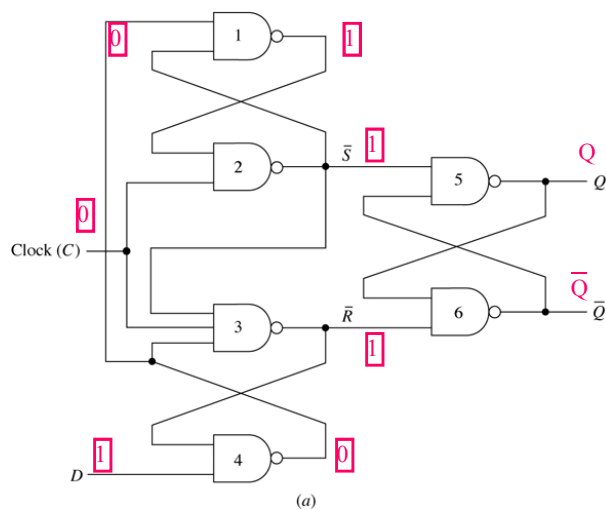
(b)



A.S.E.

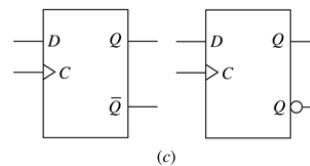
12.33

## Ck=0 , D=1 (Fine)



Inputs		Outputs	
D	C	$Q^+$	$\bar{Q}^+$
0	↑	0	1
1	↑	1	0
X	0	$Q$	$\bar{Q}$
X	1	$Q$	$\bar{Q}$

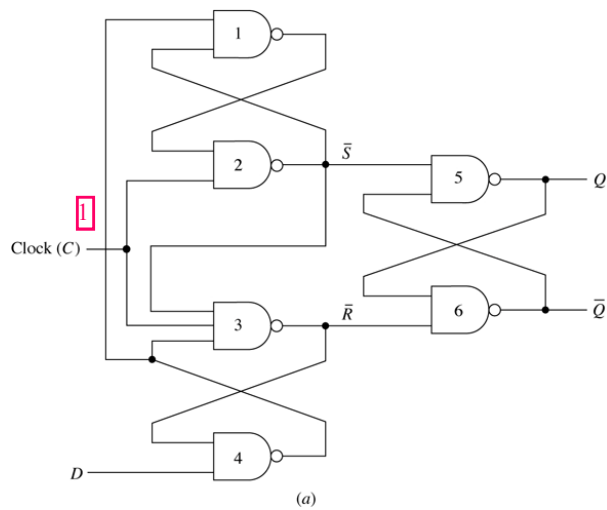
(b)



A.S.E.

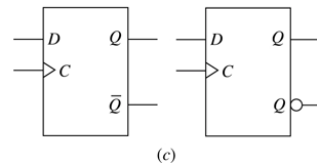
12.34

**CK=1**



Inputs		Outputs	
$D$	$C$	$Q^+$	$\bar{Q}^+$
0	$\uparrow$	0	1
1	$\uparrow$	1	0
X	0	$Q$	$\bar{Q}$
X	1	$Q$	$\bar{Q}$

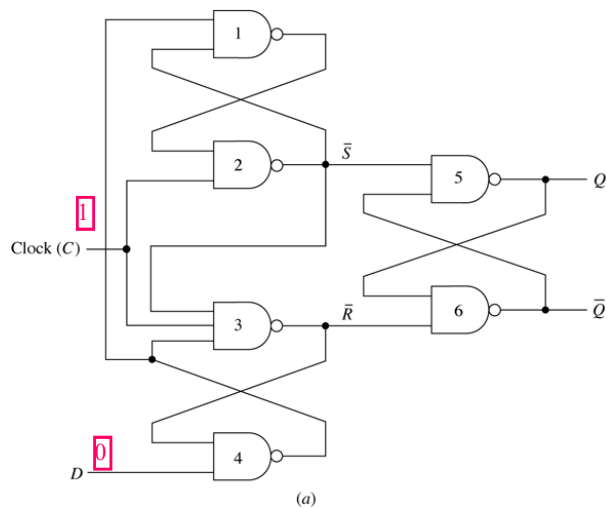
(b)



**A.S.E.**

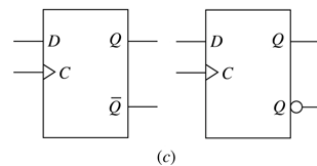
**12.35**

**Ck=1 , D=0 (1)**



Inputs		Outputs	
$D$	$C$	$Q^+$	$\bar{Q}^+$
0	$\uparrow$	0	1
1	$\uparrow$	1	0
X	0	$Q$	$\bar{Q}$
X	1	$Q$	$\bar{Q}$

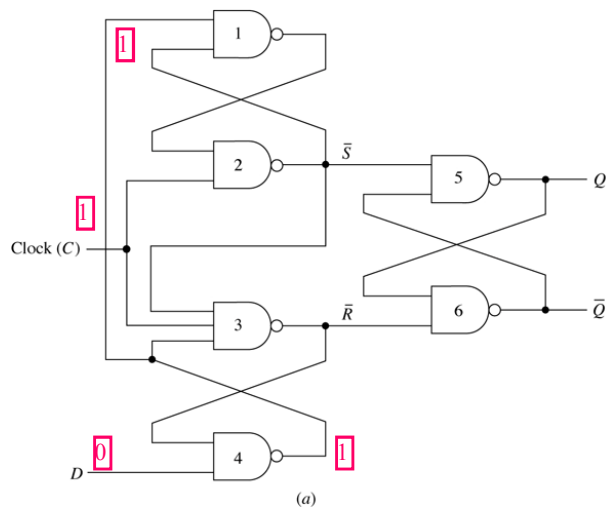
(b)



**A.S.E.**

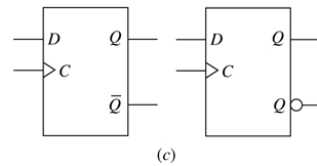
**12.36**

## Ck=1 , D=0 (2)



Inputs		Outputs	
D	C	$Q^+$	$\bar{Q}^+$
0	↑	0	1
1	↑	1	0
X	0	Q	$\bar{Q}$
X	1	Q	$\bar{Q}$

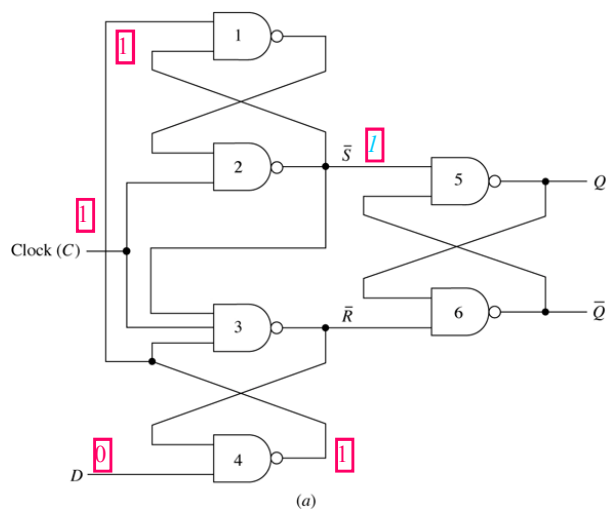
(b)



A.S.E.

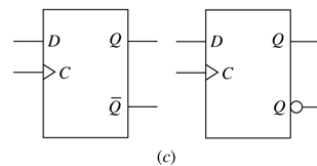
12.37

## Ck=1 , D=0 (3)



Inputs		Outputs	
D	C	$Q^+$	$\bar{Q}^+$
0	↑	0	1
1	↑	1	0
X	0	Q	$\bar{Q}$
X	1	Q	$\bar{Q}$

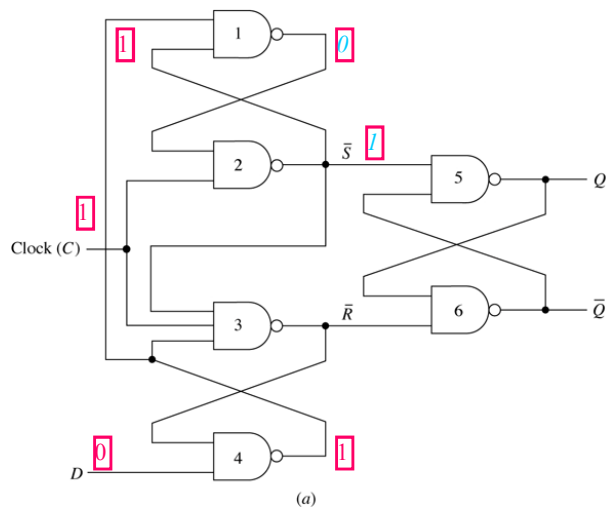
(b)



A.S.E.

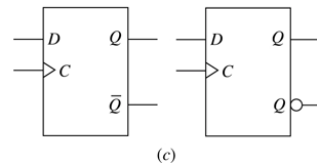
12.38

## Ck=1 , D=0 (4)



Inputs		Outputs	
D	C	$Q^+$	$\bar{Q}^+$
0	↑	0	1
1	↑	1	0
X	0	Q	$\bar{Q}$
X	1	Q	$\bar{Q}$

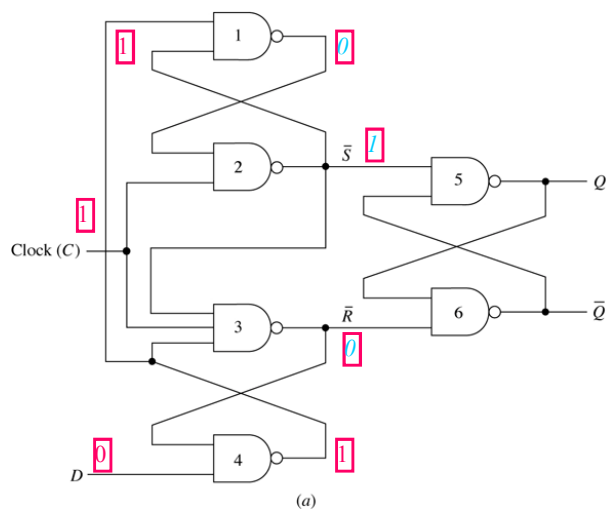
(b)



A.S.E.

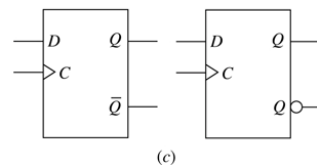
12.39

## Ck=1 , D=0 (5)



Inputs		Outputs	
D	C	$Q^+$	$\bar{Q}^+$
0	↑	0	1
1	↑	1	0
X	0	Q	$\bar{Q}$
X	1	Q	$\bar{Q}$

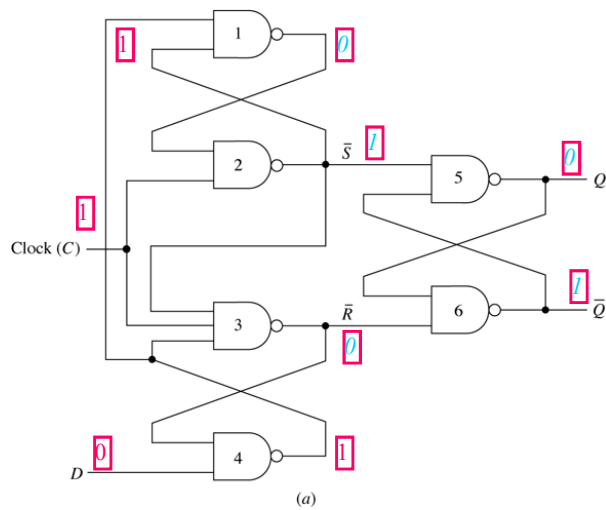
(b)



A.S.E.

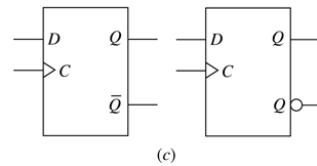
12.40

**Ck=1 , D=0 , Q=0 (Fine)**



Inputs		Outputs	
D	C	$Q^+$	$\bar{Q}^+$
0	↑	0	1
1	↑	1	0
X	0	Q	$\bar{Q}$
X	1	Q	$\bar{Q}$

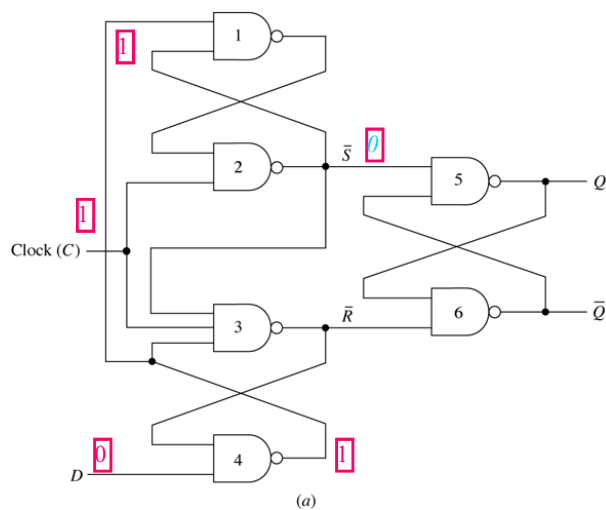
(b)



A.S.E.

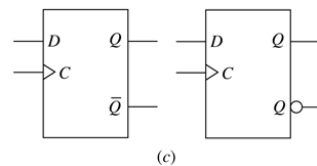
12.41

**Ck=1 , D=0 (1')**



Inputs		Outputs	
D	C	$Q^+$	$\bar{Q}^+$
0	↑	0	1
1	↑	1	0
X	0	Q	$\bar{Q}$
X	1	Q	$\bar{Q}$

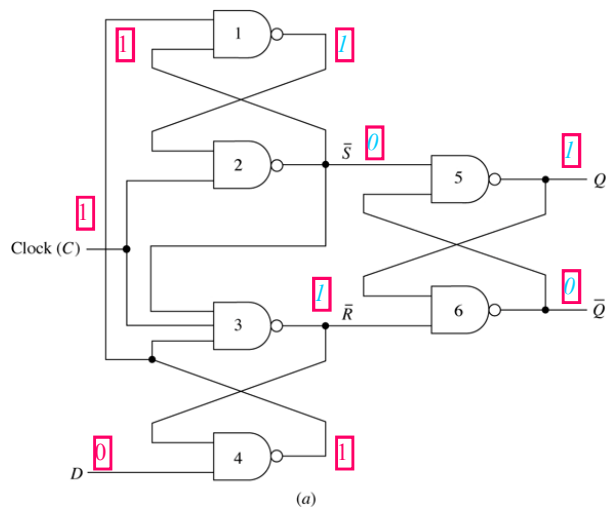
(b)



A.S.E.

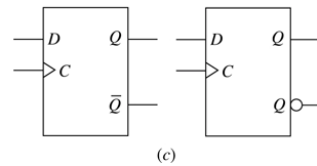
12.42

**Ck=1 , D=0 , Q=1 (Fine)**



Inputs		Outputs	
D	C	$Q^+$	$\bar{Q}^+$
0	↑	0	1
1	↑	1	0
X	0	Q	$\bar{Q}$
X	1	Q	$\bar{Q}$

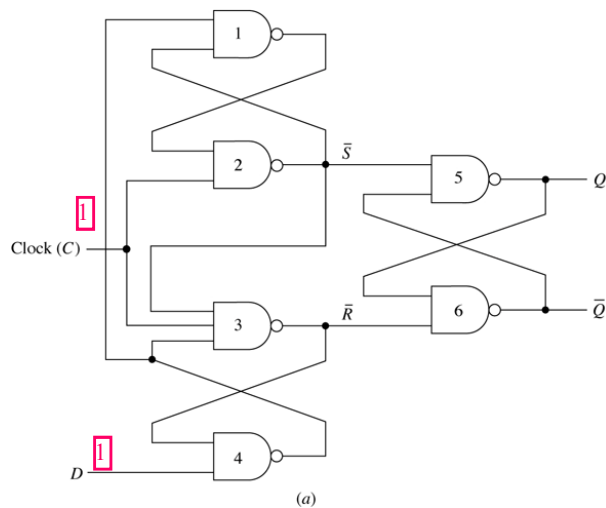
(b)



A.S.E.

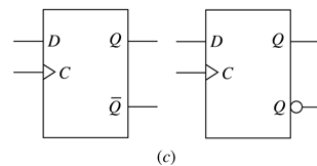
12.43

**Ck=1 , D=1 (1)**



Inputs		Outputs	
D	C	$Q^+$	$\bar{Q}^+$
0	↑	0	1
1	↑	1	0
X	0	Q	$\bar{Q}$
X	1	Q	$\bar{Q}$

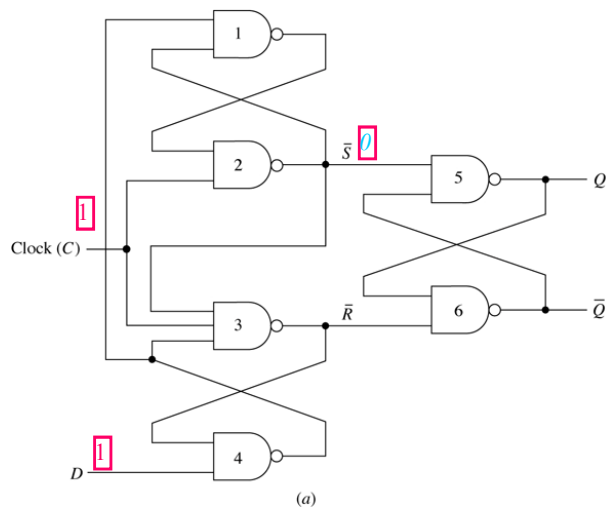
(b)



A.S.E.

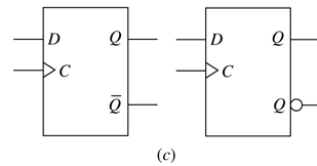
12.44

## Ck=1 , D=1 (2)



Inputs		Outputs	
D	C	$Q^+$	$\bar{Q}^+$
0	↑	0	1
1	↑	1	0
X	0	$Q$	$\bar{Q}$
X	1	$Q$	$\bar{Q}$

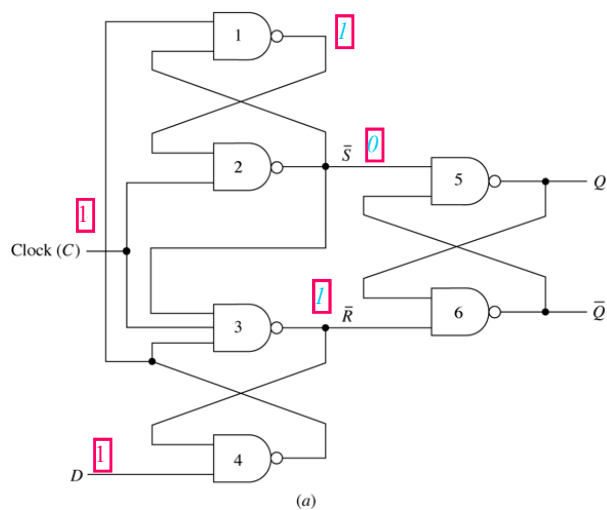
(b)



A.S.E.

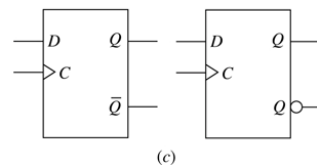
12.45

## Ck=1 , D=1 (3)



Inputs		Outputs	
D	C	$Q^+$	$\bar{Q}^+$
0	↑	0	1
1	↑	1	0
X	0	$Q$	$\bar{Q}$
X	1	$Q$	$\bar{Q}$

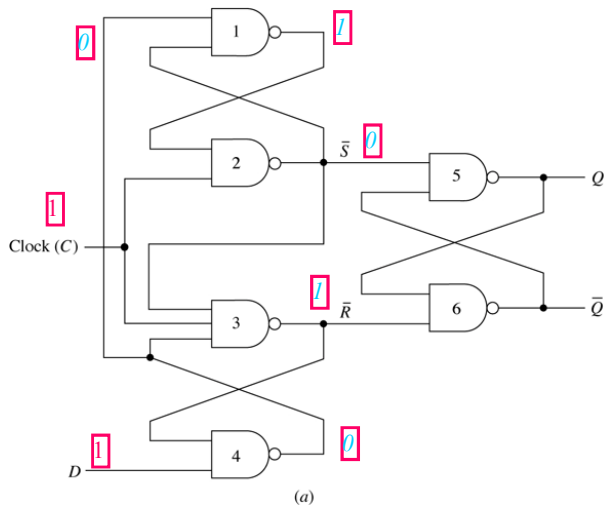
(b)



A.S.E.

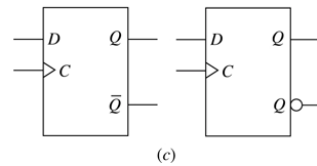
12.46

## Ck=1 , D=1 (4)



Inputs		Outputs	
D	C	$Q^+$	$\bar{Q}^+$
0	↑	0	1
1	↑	1	0
X	0	Q	$\bar{Q}$
X	1	Q	$\bar{Q}$

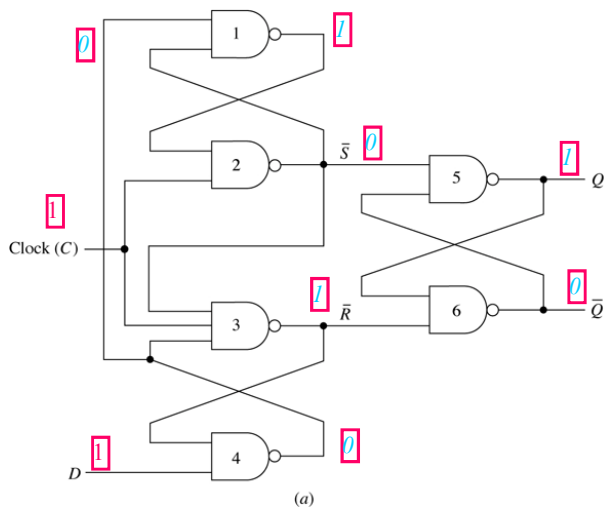
(b)



A.S.E.

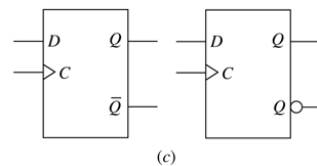
12.47

## Ck=1 , D=1 , Q=1 (Fine)



Inputs		Outputs	
D	C	$Q^+$	$\bar{Q}^+$
0	↑	0	1
1	↑	1	0
X	0	Q	$\bar{Q}$
X	1	Q	$\bar{Q}$

(b)

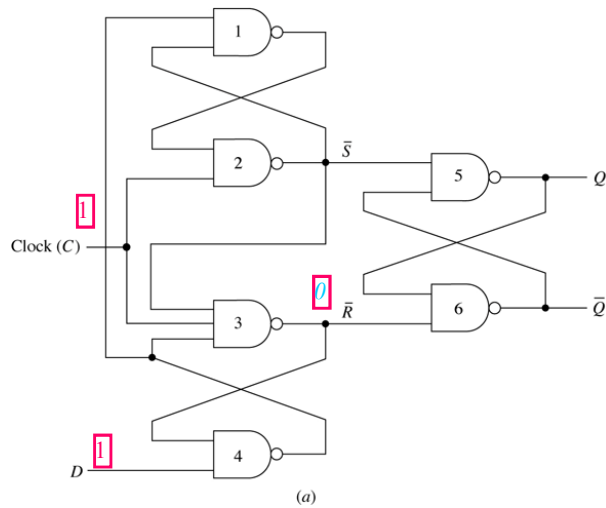


A.S.E.

12.48

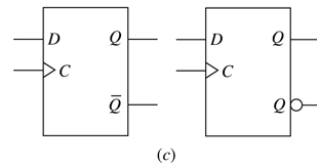


## Ck=1 , D=1 (1')



Inputs		Outputs	
D	C	$Q^+$	$\bar{Q}^+$
0	↑	0	1
1	↑	1	0
X	0	$Q$	$\bar{Q}$
X	1	$Q$	$\bar{Q}$

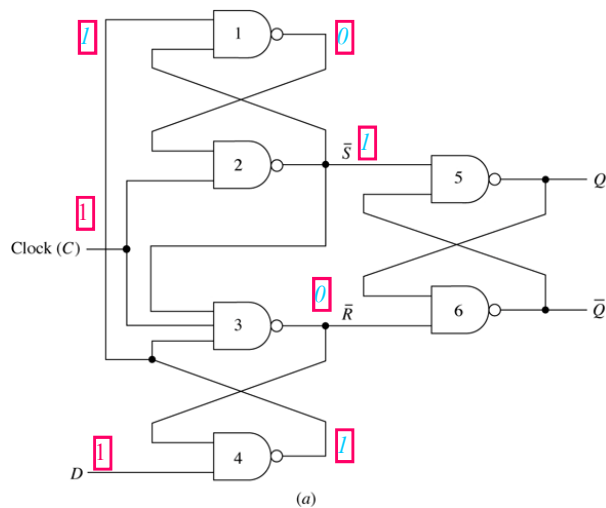
(b)



A.S.E.

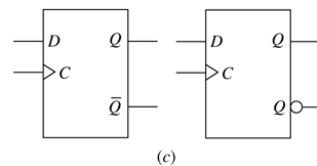
12.49

## Ck=1 , D=1 (2')



Inputs		Outputs	
D	C	$Q^+$	$\bar{Q}^+$
0	↑	0	1
1	↑	1	0
X	0	$Q$	$\bar{Q}$
X	1	$Q$	$\bar{Q}$

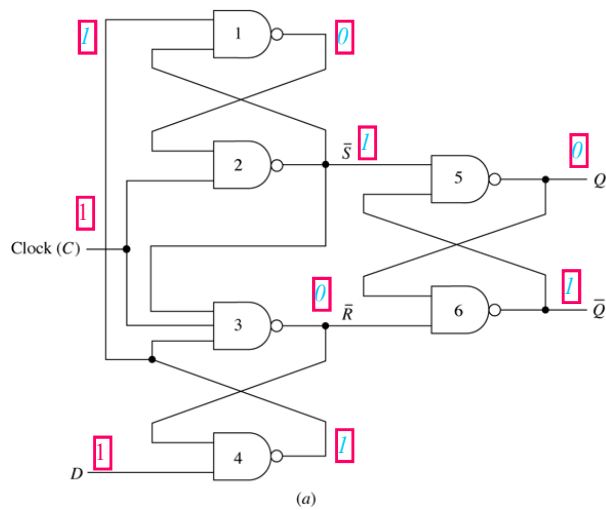
(b)



A.S.E.

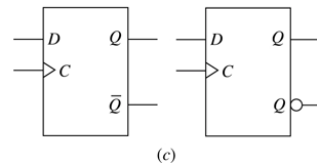
12.50

## Ck=1 , D=1 , Q=0 (Fine)



Inputs		Outputs	
D	C	$Q^+$	$\bar{Q}^+$
0	↑	0	1
1	↑	1	0
X	0	$Q$	$\bar{Q}$
X	1	$Q$	$\bar{Q}$

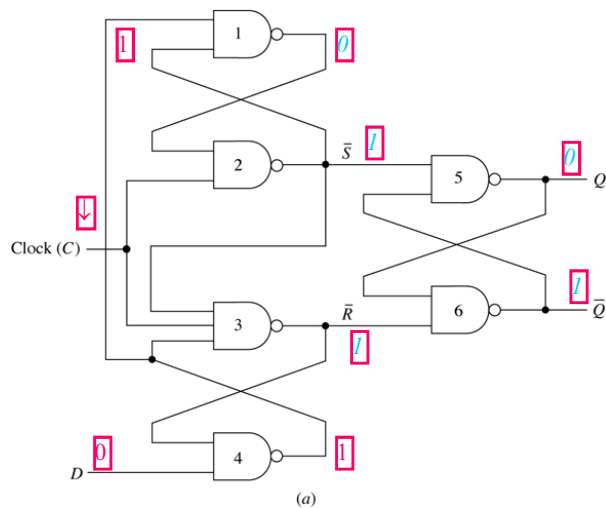
(b)



A.S.E.

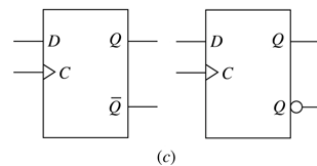
12.51

## Ck=1→0 , D=0 , Q=0 (Fine)



Inputs		Outputs	
D	C	$Q^+$	$\bar{Q}^+$
0	↑	0	1
1	↑	1	0
X	0	$Q$	$\bar{Q}$
X	1	$Q$	$\bar{Q}$

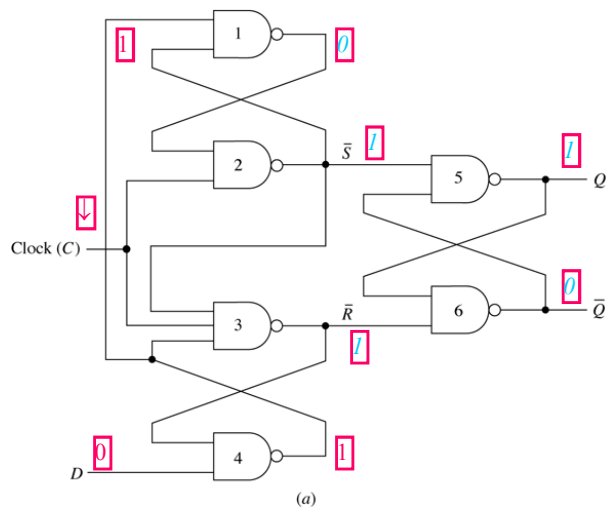
(b)



A.S.E.

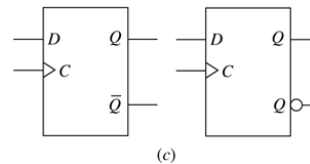
12.52

## Ck=1→0 , D=0 , Q=1 (Fine)



Inputs		Outputs	
D	C	$Q^+$	$\bar{Q}^+$
0	↑	0	1
1	↑	1	0
X	0	$Q$	$\bar{Q}$
X	1	$Q$	$\bar{Q}$

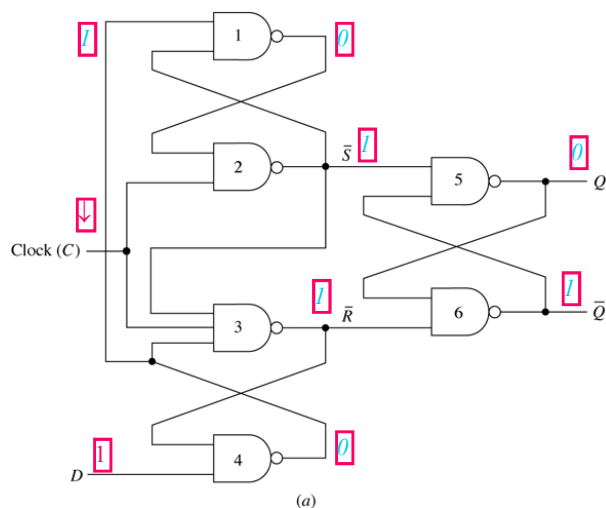
(b)



A.S.E.

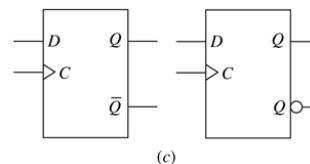
12.53

## Ck=1→0 , D=1 , Q=0 (Fine)



Inputs		Outputs	
D	C	$Q^+$	$\bar{Q}^+$
0	↑	0	1
1	↑	1	0
X	0	$Q$	$\bar{Q}$
X	1	$Q$	$\bar{Q}$

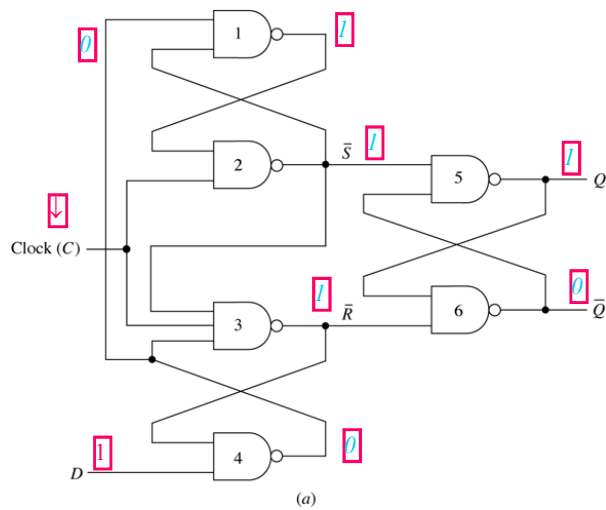
(b)



A.S.E.

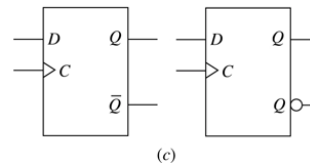
12.54

**Ck=1→0 , D=1 , Q=1 (Fine)**



Inputs		Outputs	
D	C	$Q^+$	$\bar{Q}^+$
0	↑	0	1
1	↑	1	0
X	0	$Q$	$\bar{Q}$
X	1	$Q$	$\bar{Q}$

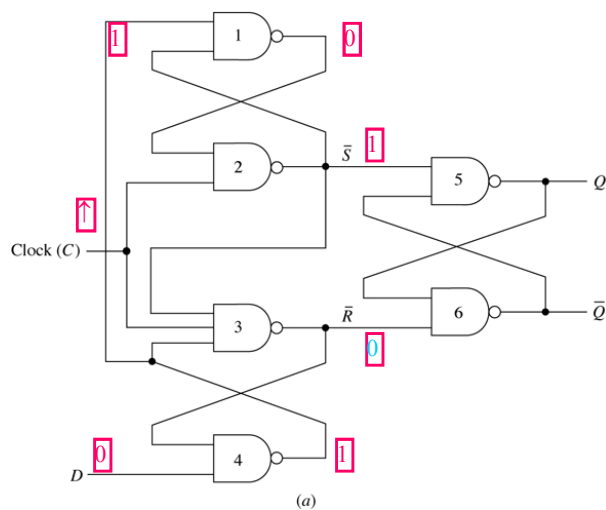
(b)



A.S.E.

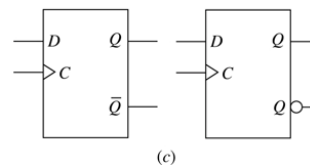
12.55

**Ck=0→1 , D=0 (1)**



Inputs		Outputs	
D	C	$Q^+$	$\bar{Q}^+$
0	↑	0	1
1	↑	1	0
X	0	$Q$	$\bar{Q}$
X	1	$Q$	$\bar{Q}$

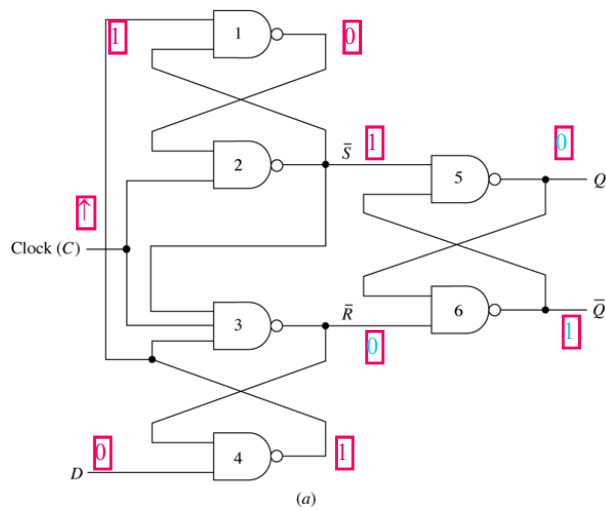
(b)



A.S.E.

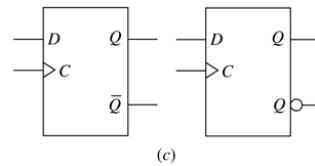
12.56

## Ck=0→1 , D=0 , Q=0 (Fine)



Inputs		Outputs	
D	C	$Q^+$	$\bar{Q}^+$
0	↑	0	1
1	↑	1	0
X	0	$Q$	$\bar{Q}$
X	1	$Q$	$\bar{Q}$

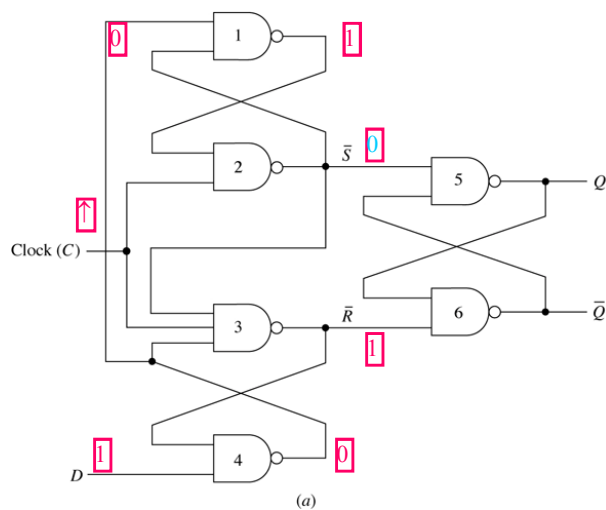
(b)



A.S.E.

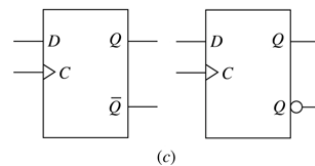
12.57

## Ck=0→1 , D=1 (1)



Inputs		Outputs	
D	C	$Q^+$	$\bar{Q}^+$
0	↑	0	1
1	↑	1	0
X	0	$Q$	$\bar{Q}$
X	1	$Q$	$\bar{Q}$

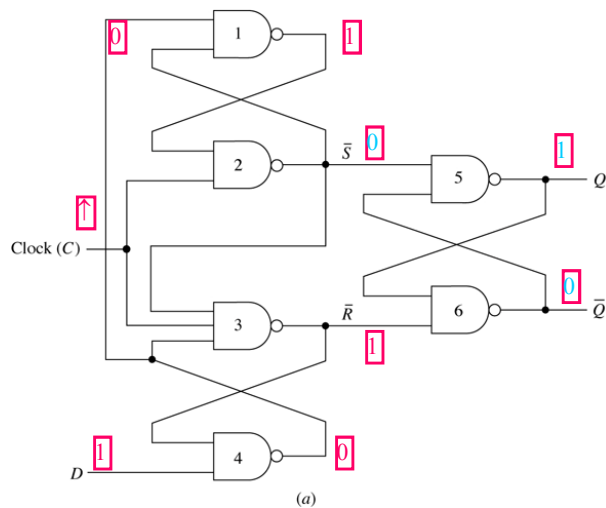
(b)



A.S.E.

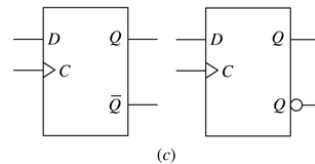
12.58

## Ck=0→1 , D=1 , Q=1 (Fine)



Inputs		Outputs	
D	C	$Q^+$	$\bar{Q}^+$
0	↑	0	1
1	↑	1	0
X	0	Q	$\bar{Q}$
X	1	Q	$\bar{Q}$

(b)



(c)

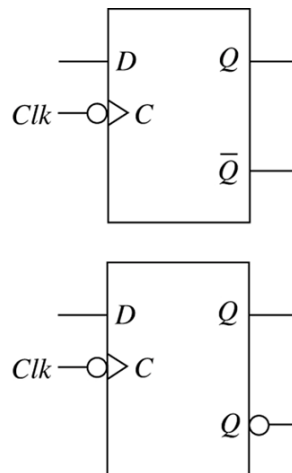
A.S.E.

12.59

## D Negative Edge Triggered

Inputs		Outputs	
D	Clk	$Q^+$	$\bar{Q}^+$
0	↓	0	1
1	↓	1	0
X	0	Q	$\bar{Q}$
X	1	Q	$\bar{Q}$

(a)



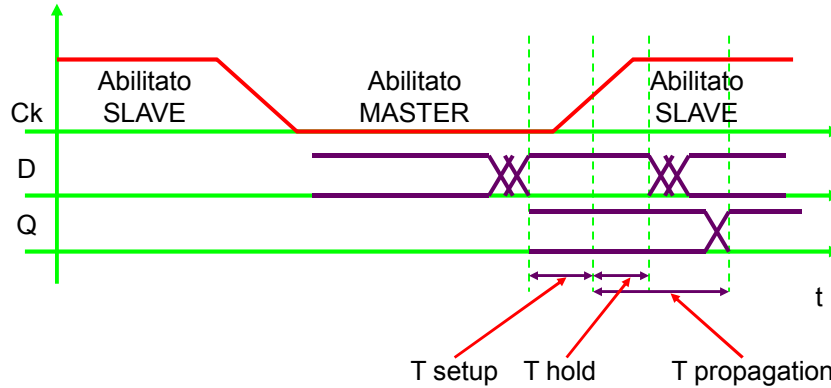
(b)

A.S.E.

12.60

## Tempi di Rispetto

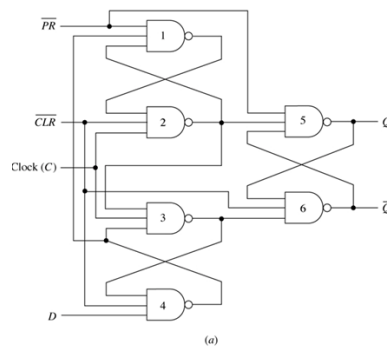
- Per evitare errori in fase di memorizzazione è necessario che il dato sia stabile un po' prima e un po' dopo la commutazione del clock



A.S.E.

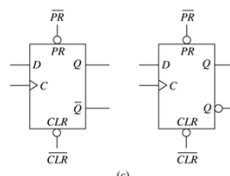
12.61

## D Edge Triggered con Preset e Clear Asincroni



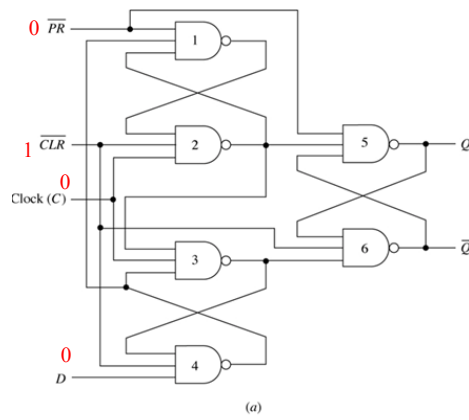
Inputs				Outputs	
PR	CLR	D	C	Q*	Q*
0	1	X	X	1	0
1	0	X	X	0	1
0	0	X	X	1*	1*
1	1	0	↑	0	1
1	1	1	↑	1	0
1	1	X	0	Q	Q
1	1	X	1	Q	Q

\*Unpredictable behavior will result if PR and CLR return to 1 simultaneously



A.S.E.

12.62



Inputs				Outputs	
$\overline{PR}$	$\overline{CLR}$	$D$	$C$	$Q^+$	$\overline{Q}^+$
0	1	X	X	1	0
1	0	X	X	0	1
0	0	X	X	1*	1*
1	1	0	↑	0	1
1	1	1	↑	1	0
1	1	X	0	$Q$	$\overline{Q}$
1	1	X	1	$Q$	$\overline{Q}$

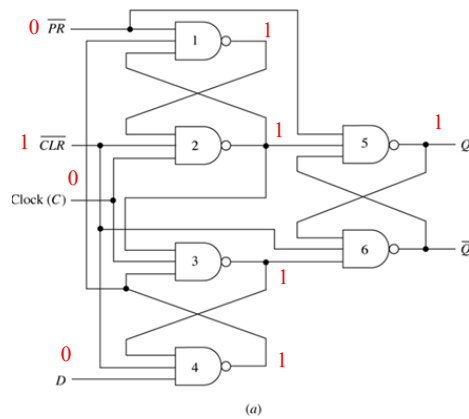
\*Unpredictable behavior will result if  $\overline{PR}$  and  $\overline{CLR}$  return to 1 simultaneously

(b)

**$\overline{PR} = 0, CK = 0, D = 0 (1)$**

A.S.E.

12.63



Inputs				Outputs	
$\overline{PR}$	$\overline{CLR}$	$D$	$C$	$Q^+$	$\overline{Q}^+$
0	1	X	X	1	0
1	0	X	X	0	1
0	0	X	X	1*	1*
1	1	0	↑	0	1
1	1	1	↑	1	0
1	1	X	0	$Q$	$\overline{Q}$
1	1	X	1	$Q$	$\overline{Q}$

\*Unpredictable behavior will result if  $\overline{PR}$  and  $\overline{CLR}$  return to 1 simultaneously

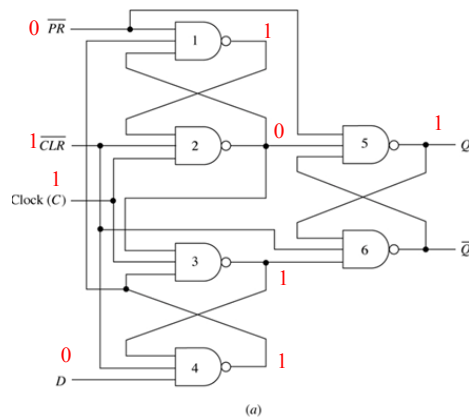
(b)

**$\overline{PR} = 0, CK = 0, D = 0 (2)$**

A.S.E.

12.64





Inputs				Outputs	
$\overline{PR}$	$\overline{CLR}$	$D$	$C$	$Q^+$	$\overline{Q}^+$
0	1	X	X	1	0
1	0	X	X	0	1
0	0	X	X	1*	1*
1	1	0	↑	0	1
1	1	1	↑	1	0
1	1	X	0	$Q$	$\overline{Q}$
1	1	X	1	$Q$	$\overline{Q}$

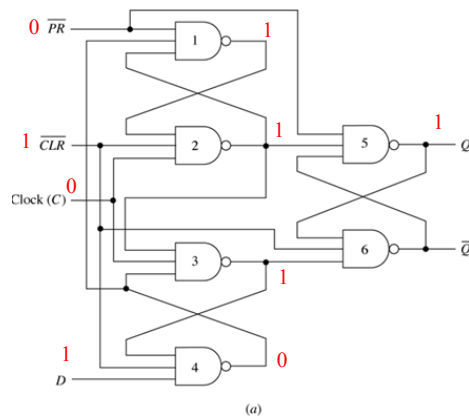
\*Unpredictable behavior will result if  $\overline{PR}$  and  $\overline{CLR}$  return to 1 simultaneously

(b)

**$\overline{PR} = 0$  ,  $CK = 1$  ,  $D = 0$**

A.S.E.

12.65



Inputs				Outputs	
$\overline{PR}$	$\overline{CLR}$	$D$	$C$	$Q^+$	$\overline{Q}^+$
0	1	X	X	1	0
1	0	X	X	0	1
0	0	X	X	1*	1*
1	1	0	↑	0	1
1	1	1	↑	1	0
1	1	X	0	$Q$	$\overline{Q}$
1	1	X	1	$Q$	$\overline{Q}$

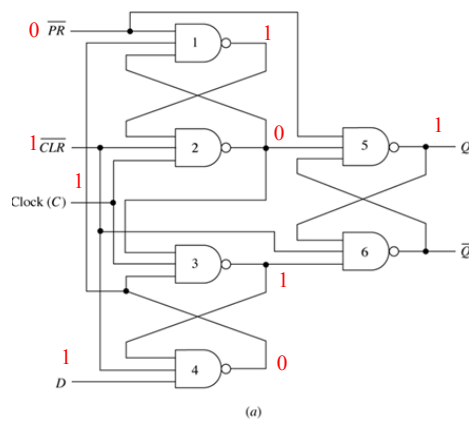
\*Unpredictable behavior will result if  $\overline{PR}$  and  $\overline{CLR}$  return to 1 simultaneously

(b)

**$\overline{PR} = 0$  ,  $CK = 0$  ,  $D = 1$**

A.S.E.

12.66



Inputs				Outputs	
$\overline{PR}$	$\overline{CLR}$	$D$	$C$	$Q^+$	$\overline{Q}^+$
0	1	X	X	1	0
1	0	X	X	0	1
0	0	X	X	1*	1*
1	1	0	↑	0	1
1	1	1	↑	1	0
1	1	X	0	$Q$	$\overline{Q}$
1	1	X	1	$Q$	$\overline{Q}$

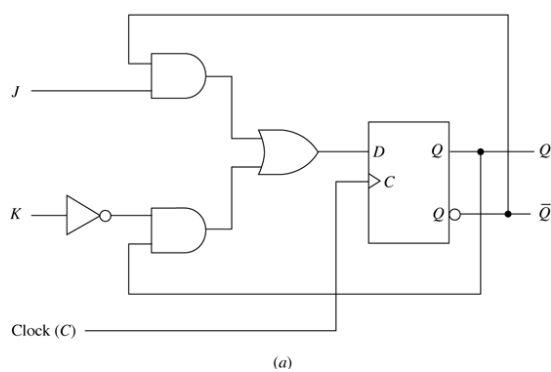
\*Unpredictable behavior will result if  $\overline{PR}$  and  $\overline{CLR}$  return to 1 simultaneously

**$\overline{PR} = 0$  ,  $CK = 1$  ,  $D = 1$**

A.S.E.

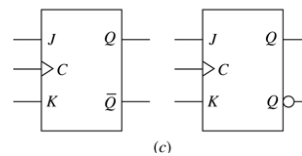
12.67

## Flip-flop J-K Positive Edge triggered (soluzione alternativa)



Inputs			Outputs	
$J$	$K$	$C$	$Q^+$	$\overline{Q}^+$
0	0	↑	$Q$	$\overline{Q}$
0	1	↑	0	1
1	0	↑	1	0
1	1	↑	$\overline{Q}$	$Q$
X	X	0	$Q$	$\overline{Q}$
X	X	1	$Q$	$\overline{Q}$

(b)

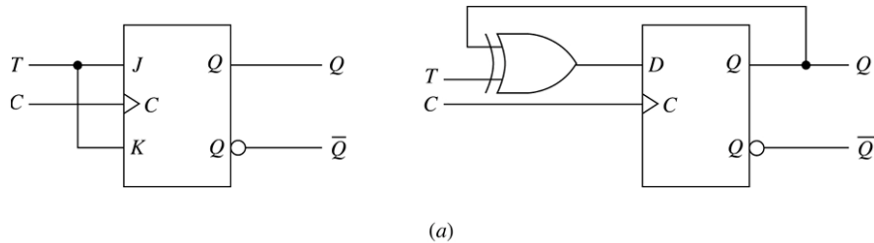


(c)

A.S.E.

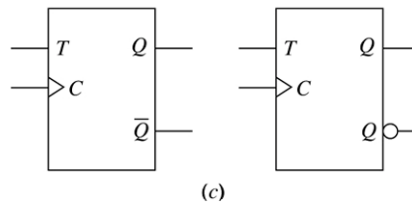
12.68

## Flip-flop T Positive Edge triggered (soluzione alternativa)



Inputs		Outputs	
$T$	$C$	$Q^+$	$\bar{Q}^+$
0	$\uparrow$	$Q$	$\bar{Q}$
1	$\uparrow$	$\bar{Q}$	$Q$
X	0	$Q$	$\bar{Q}$
X	1	$Q$	$\bar{Q}$

(b)



A.S.E.

12.69

## Conclusioni

- Architettura MASTER – SLAVE
- Clock a 2 fasi
- Flip-flop J – K master-slave
- D Master - Slave
- T Master – Slave
- Flip-flop D Edge triggered
- Tempi di rispetto
- Soluzioni alternative

A.S.E.

12.70